UNIVERSITY OF CAMBRIDGE

SPINTRONIC LOGIC

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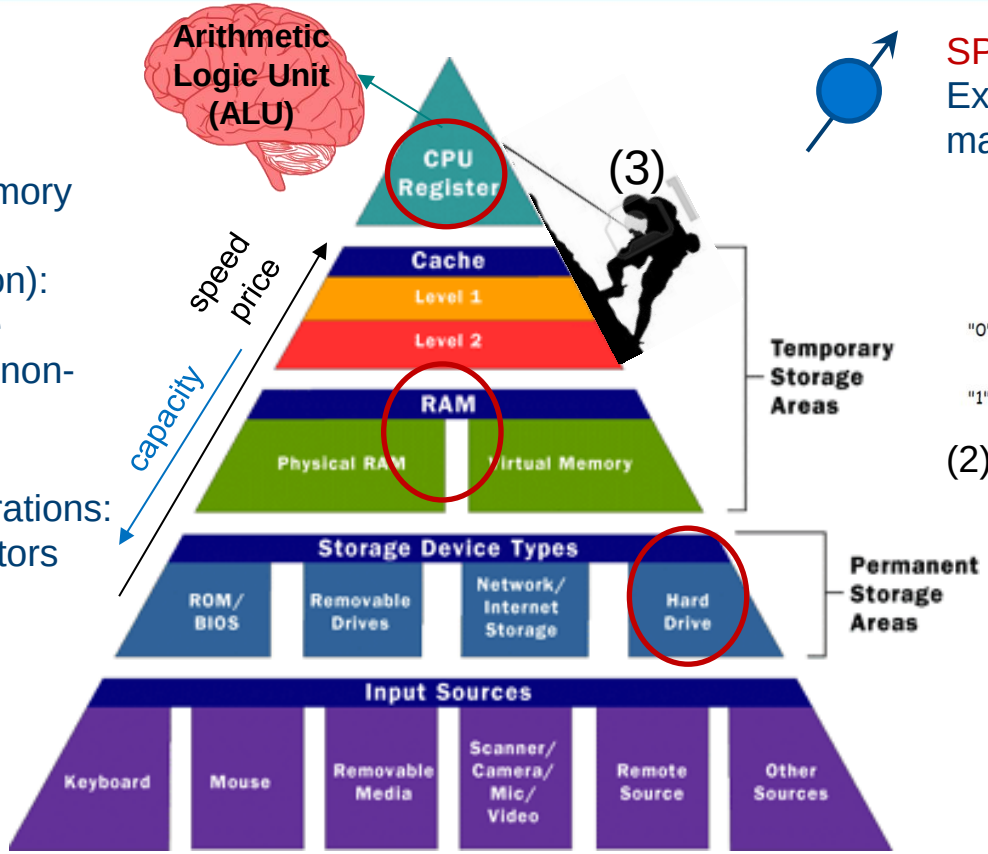
Novel frontiers in Magnetism. 14th of February, Benasque

Computer memory architecture

Traditionally, computer memory divided between:

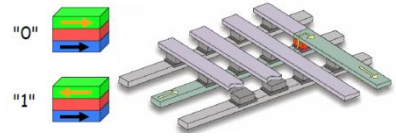
- Transistor-based (Silicon): fast, volatile, expensive
- Magnetic-based: Slow, non-volatile, cheap

Computational & logic operations: All performed using transistors

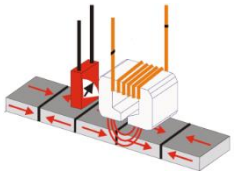


howstuffworks.com

SPINTRONICS:
Exploiting both charge & magnetism of electron

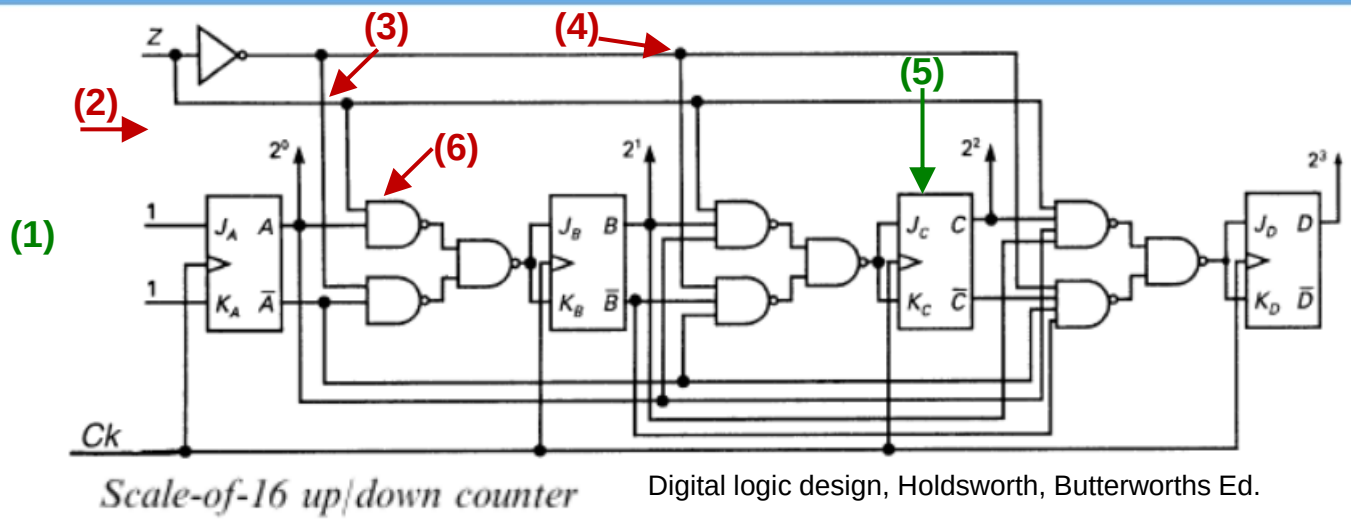


(2) MRAM based on MTJs



(1) GMR sensors

Can spintronic circuits do this?



Digital logic design, Holdsworth, Butterworths Ed.

1. Device based on non-linear response characteristics
2. Dataflow between devices in a well-defined direction
3. Cross-over between circuit lines
4. Signal copy: fan-out
5. Sequential logic → data storage
6. Need of a full set of logic gates:
   a) INVERSION (NOT) & COMPARISON (AND/OR)
   b) NAND & NOR

+

Better or at least similar performance than transistors:

Speed, miniaturisation, design simplicity, cost, power consumption

Outline

1. Coupled nanomagnets (nano-magnetic logic)
2. Domain-walls in nanowires
3. MRAM & CMOS

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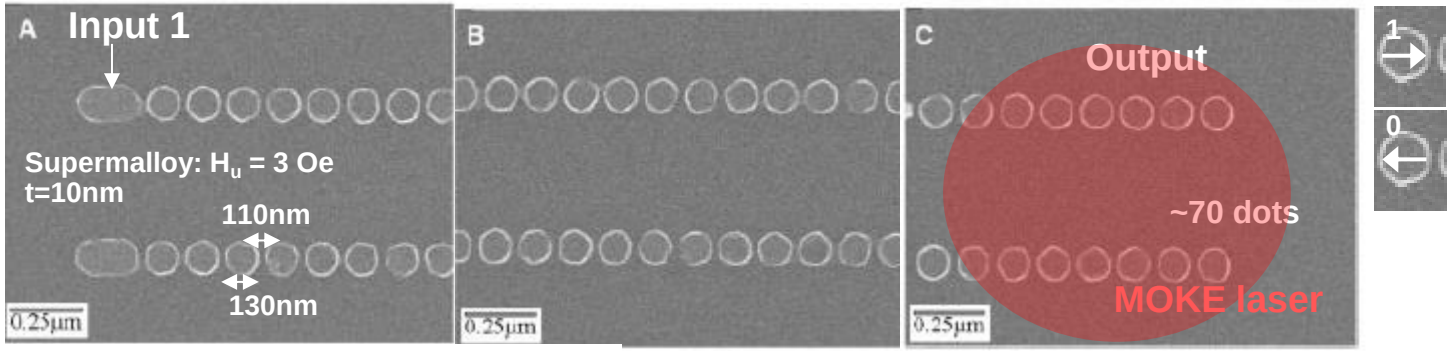
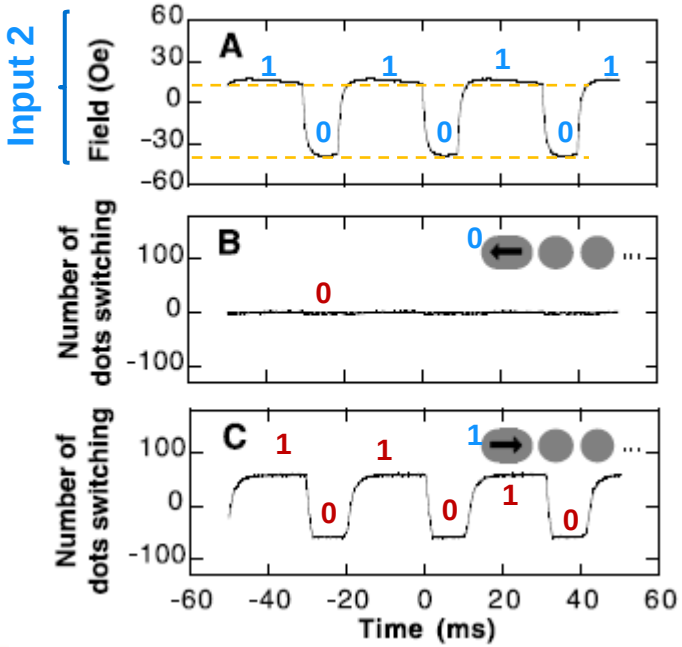
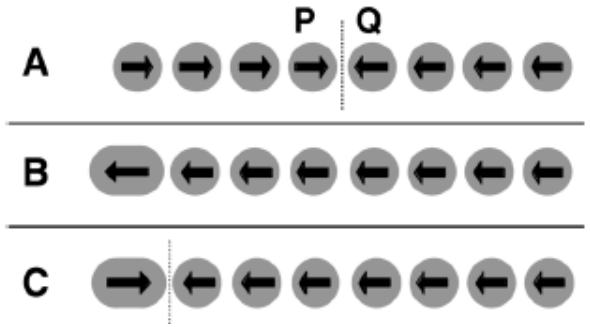
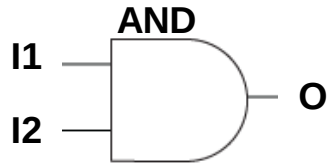
2. Domain-walls in nanowires
3. MRAM & CMOS

Dipolar interactions between nanomagnets







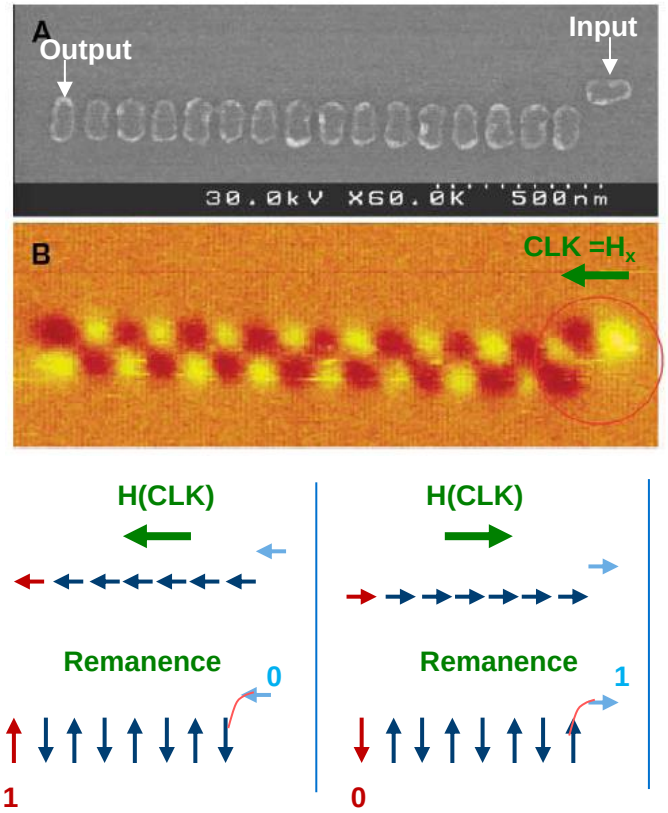


Dipolar coupling between nanomagnets (> H_u):

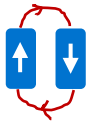
"Cascade-like" transmission of information @ RT: soliton propagation (field offset)

[Cowburn et al, Science 287, 1466 (2000)]

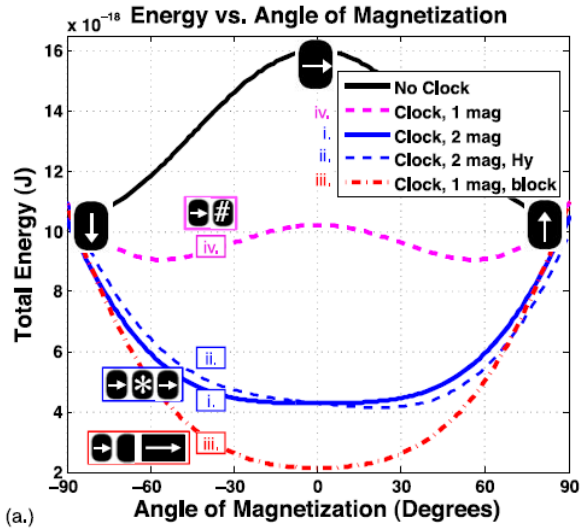
AF coupling & adiabatic switching



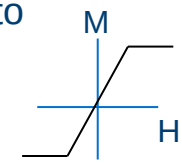
Interaction: hundreds of k_BT



Material & shape dependent



Adiabatic switching through a null state to minimise dissipation (field along HA):

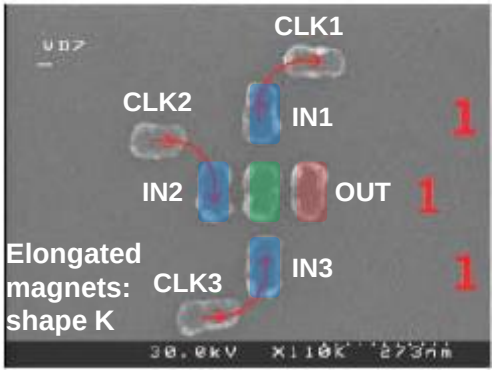


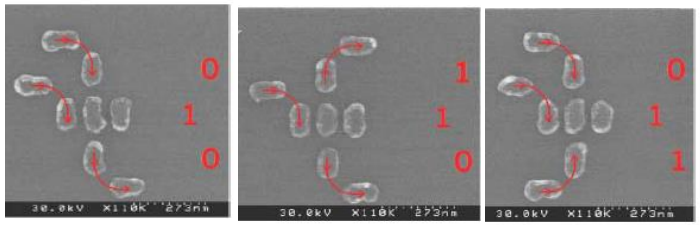
- Lower E barriers (erase)
- Inputs are applied (write)
- Walls are raised adiabatically: GND state reached (read)

Same procedure as Quantum Cellular Automata

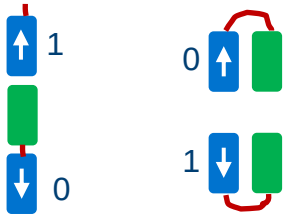
[Imre et al, Science 287, 1466 (2005) ;
Niemier et al, J. Phys.: Condens. Matter 23 493202 (2011)]

Majority gate





Input values defined by state produced in the central magnet



Logic state of input magnets	Logic state of central magnet	Logic state of output magnet
000	0	1
001	0	1
010	0	1
011	1	0
100	0	1
101	1	0
110	1	0
111	1	0

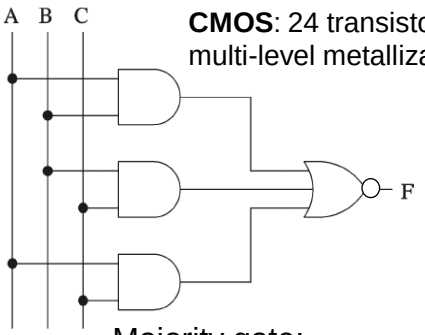
Central magnet surrounded by other 4:

- 3 inputs, driven by 3 CLK magnets
- 1 output: state determined by central magnet

Equal FM & AF coupling between magnets: Output determined by majority of inputs

25% of gates properly working

Design based on different arrangement for different inputs: new design needs to change input states independently: address inputs & outputs electrically



CMOS: 24 transistors + multi-level metallization

Majority gate:

- I2 fixed = 0 ➔ OR
- I2 fixed = 1 ➔ AND

[Imre et al, Science 287, 1466 (2005)]

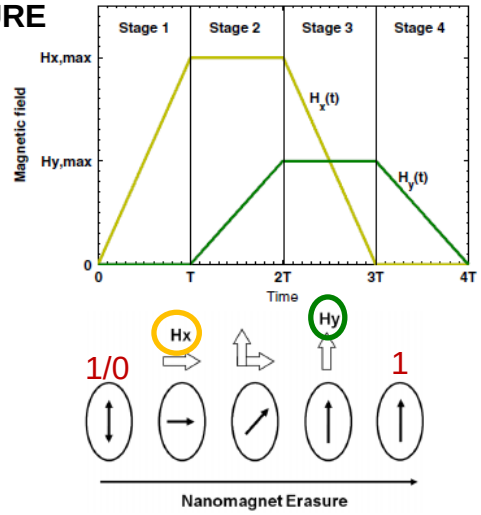
Landauer limit

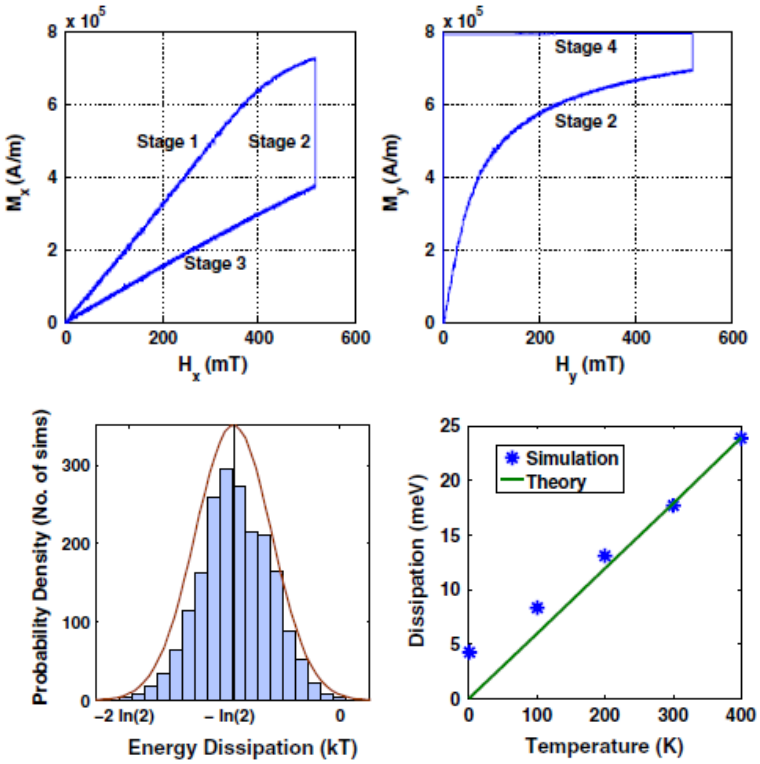
Landauer limit theorem (1961):

Any logical irreversible manipulation of information: bit erasing/merging of two computational paths → Energy consumption, $E_{min} = k_B T \ln 2$ (=2.85 zJ = 17.8 meV)

- In Semiconductor electronics: much higher losses, due to resististors & charge leakage ($V_{high} \neq V_{low}$)
- In NML should be much lower: two states degenerate E, reversal occurs via reversible uniform rotation of M

ERASURE





Computation of E consumed to erase bit (H_x & H_y) for magnet with Ms = 800 emu/cm^3, Ø=10 nm, t =2 nm, $E_k = 10k_BT$ at RT.

<E> = Landauer limit.

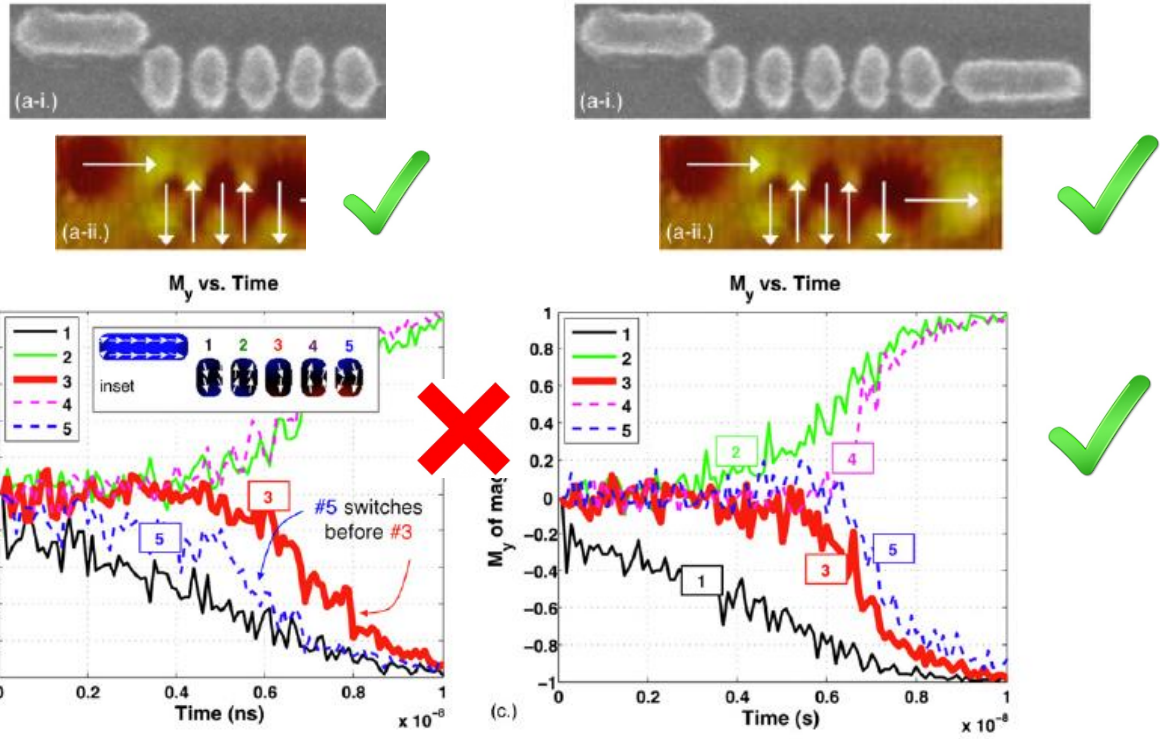
[Lambson et al, PRL 107, 010604 (2011)]

Directionality errors

STRUCTURE

FINAL STATE

TIME EVOLUTION



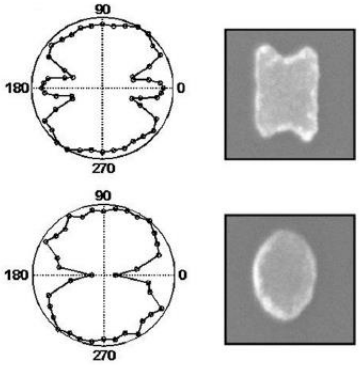
Anisotropy variations from magnet–to-magnet + thermal fluctuations: magnet along HA relaxes along EA before deterministic switching caused by H_{dip} from neighbours

SOLUTIONS: shape engineering, 4-fold anisotropy, multi-phase CLK

Output error for large N

[Niemier et al, J. Phys.: Condens. Matter 23 493202 (2011)]

4-fold anisotropy

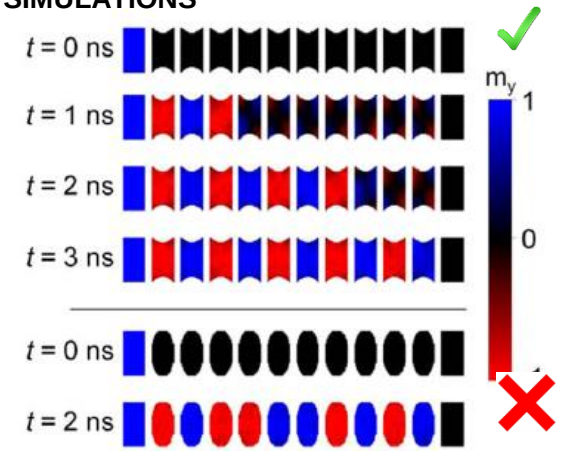


Configurational anisotropy: 4-fold anisotropy

Non-uniform magnetisation state creates higher order K

[Cowburn, J. Phys. D, Appl. Phys (2000)]

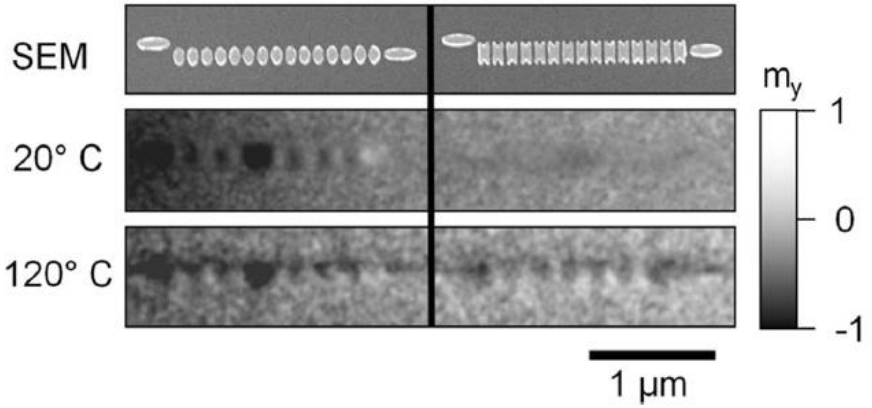
SIMULATIONS



Concave magnets have lower error rate than ellipsoidal ones:

Metastable state along x-direction: flipping only when left neighbour does

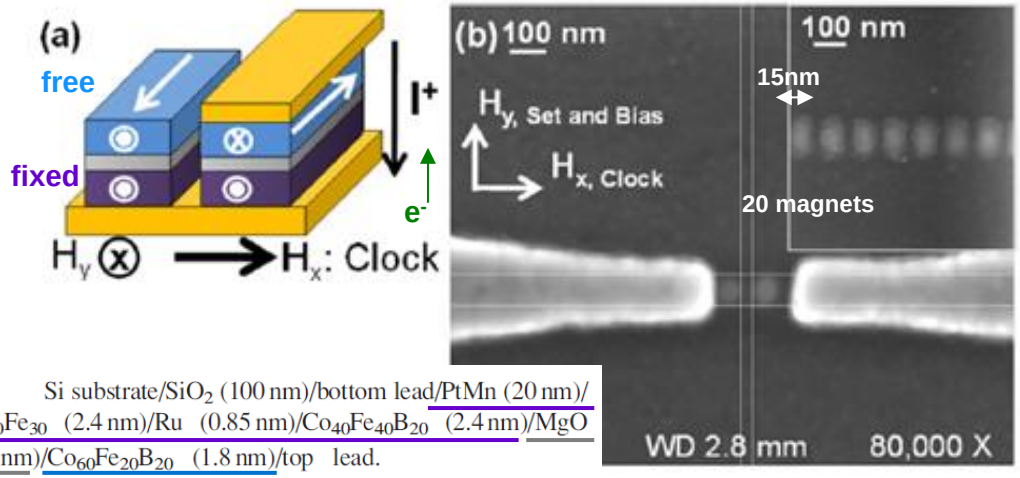
PEEM EXPERIMENTS



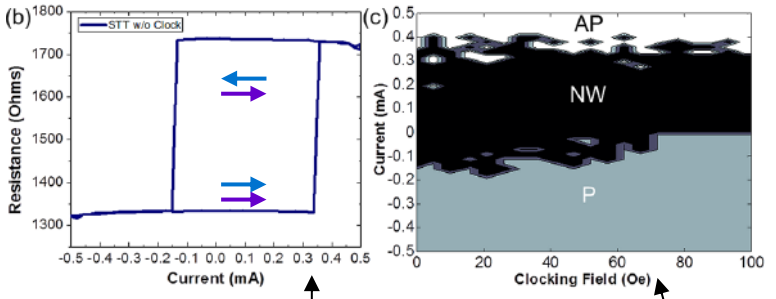
Correct propagation along 7 nanomagnets correct spacing and magnet dimensions

[Lambson et al, Appl. Phys. Lett. 100, 152406 (2012); Carlton et al, Nano Lett. 8, 4173 (2008)]

STT programming & MR readout

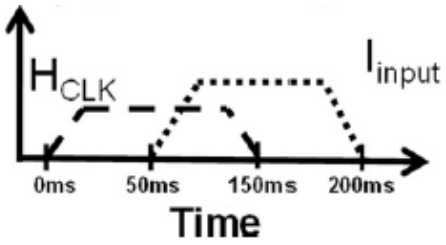


Si substrate/SiO_2 (100 nm)/bottom lead/PtMn (20 nm)/ $Co_{70}Fe_{30}$ (2.4 nm)/Ru (0.85 nm)/$Co_{40}Fe_{40}B_{20}$ (2.4 nm)/MgO (0.9 nm)/$Co_{60}Fe_{20}B_{20}$ (1.8 nm)/top lead.



Bias due to higher efficiency of one STT process with respect to the other. H_{dip} compensated

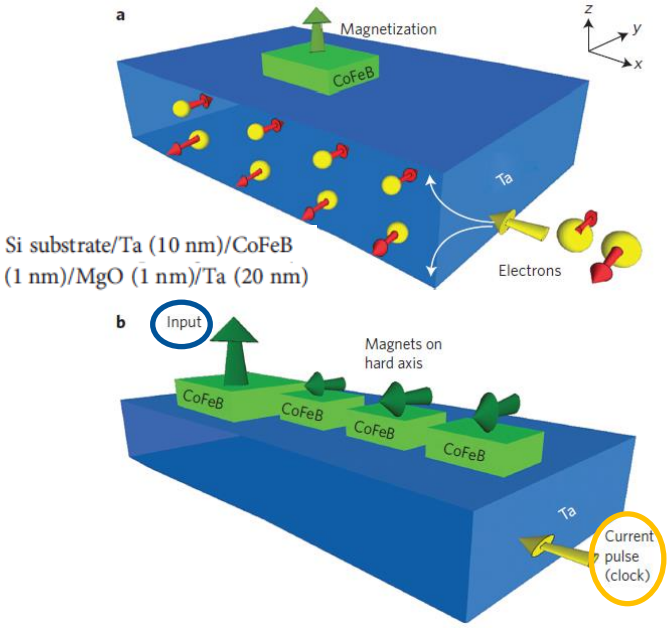
Lowers effective barrier for switching

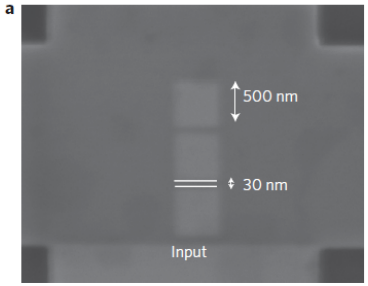


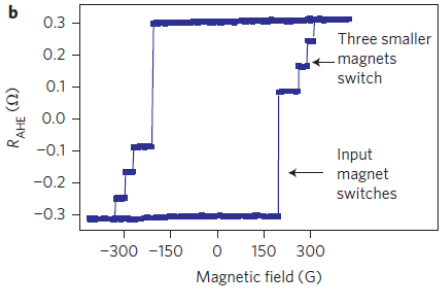
1) H_{CLK} //HA: M along x
2) H_{CLK} + I_{input}: Program the input bit
3) Neighbouring elements follow the input: data propagation & processing
4) Readout of individual magnet via TMR

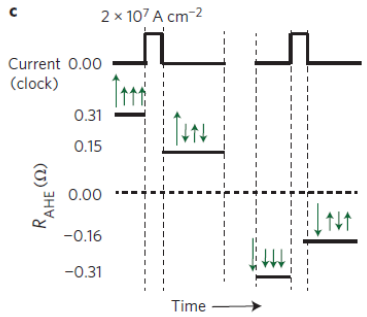
[Lyle et al, J. Appl. Phys. Lett. 100, 012402 (2012)]

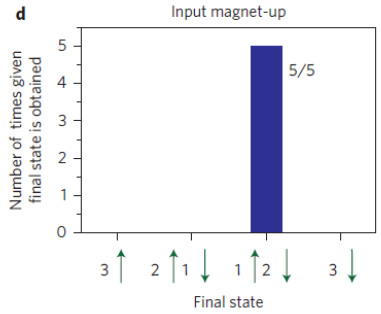
SHE clocking

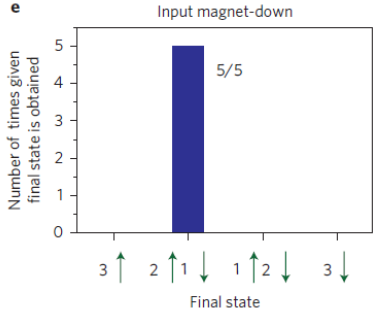










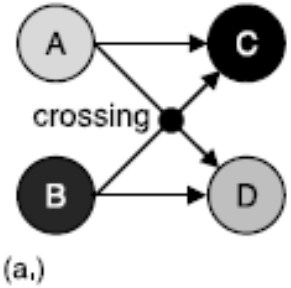


1) Unpolarised I_{CLK} : sets magnets in a metastable (IP) state via the SHE (in-plane torque created by current flowing through Ta)
2) Input sets the chain state deterministically

I_{CLK} instead of H_{CLK}:
10^3-10^4 more E efficient

[Bhowmik et al, Nat. Nano. 9, 59 (2014)]

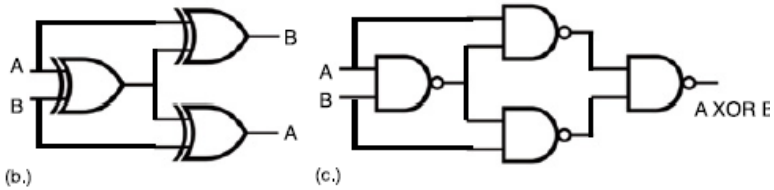
Problems: Cross-over



CMOS: Two layers of metals: Relatively simple

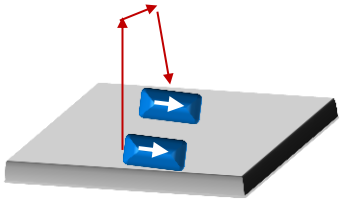
Dipolar nanomagnets: complicated

Solution 1: Alternative circuit design



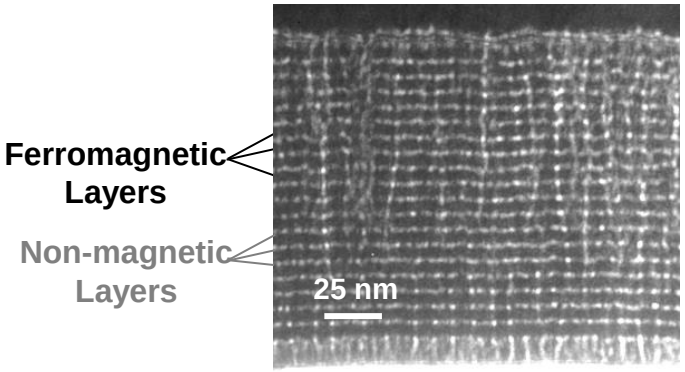
Solution 2: Middle magnet with M in diagonal

Solution 3: Information transport along the OOP direction

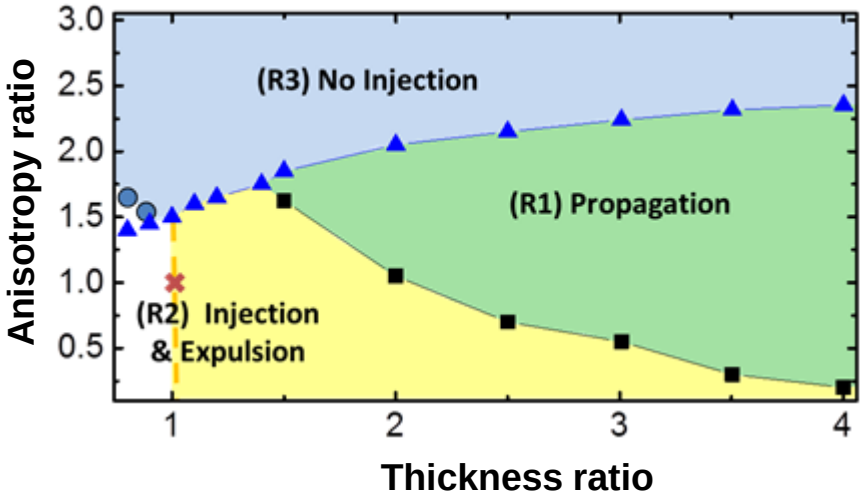


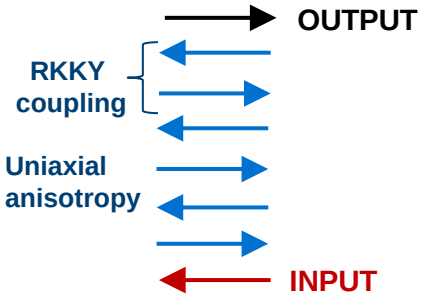
[Niemier et al, J. Phys.: Condens. Matter 23 493202 (2011)]

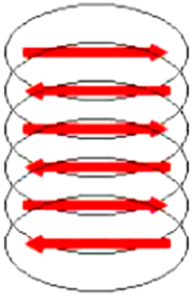
Propagation of information in vertical direction

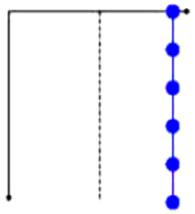


Metallic superlattice







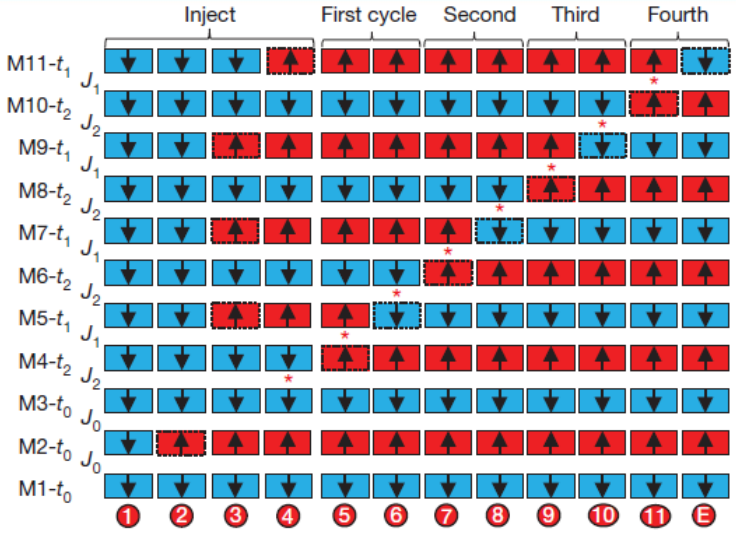


Information is propagated between layers using RKKY interactions

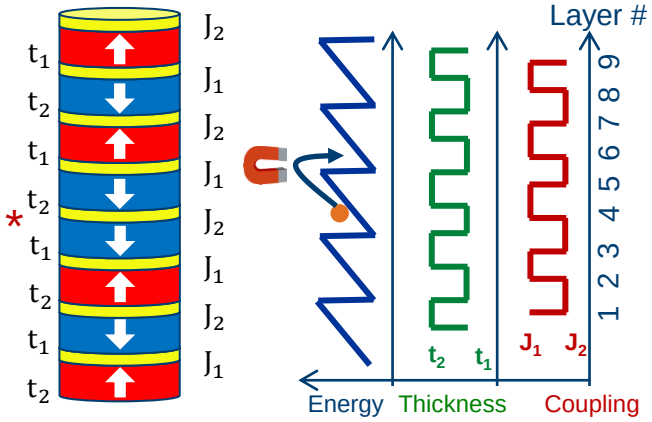
Input properties are varied to inject & propagate a soliton using external H

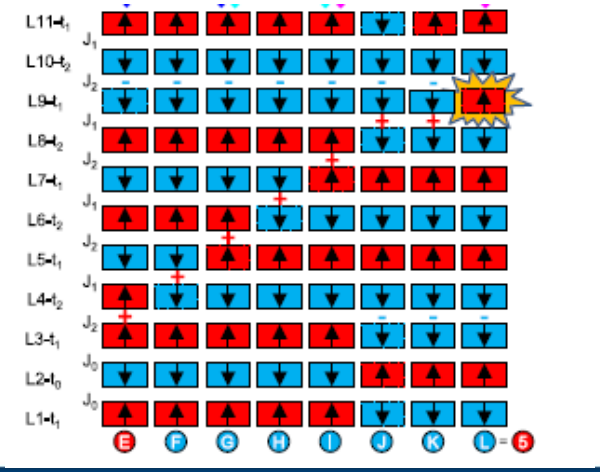
[Fernandez-Pacheco et al, Phys. Rev. B 5, 266 (2012)]

3D shift register & logic operations



STATES								
4	5	6	7	8	9	10	11	E
0	0	0	0	0	0	0	1	0
0	0	0	0	0	0	1	0	0
0	0	0	0	0	1	0	0	0
0	0	0	0	1	0	0	0	0
0	0	0	1	0	0	0	0	0
0	0	1	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0





STATES							
E	F	G	H	I	J	K	L
0	0	0	0	0	1	0	0
1	1	1	1	1	1	1	0
0	0	0	0	0	1	1	0
0	0	0	0	1	0	0	0
0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	0
0	1	0	0	0	0	0	0
1	0	0	0	0	1	1	1

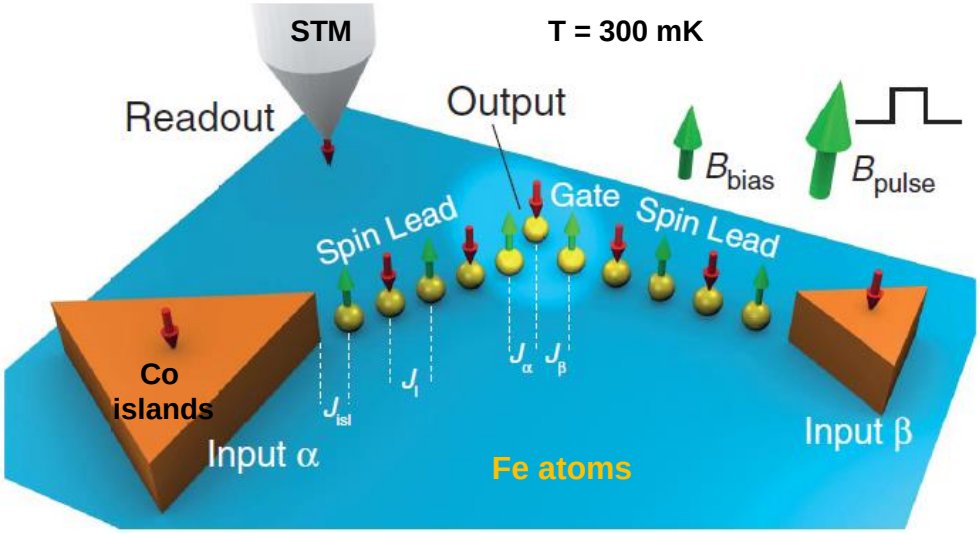
Periodic coupling & thickness: ratchet E profile for soliton propagation:

- Synchronous propagation of information with external field
- Logic operations based on solitons annihilation

Electronic functionality of tens of transistors within vertical length ~2 nm

[Lavrijsen et al, Nature 493, 647 (2013); Nanotechnology in press (2014)]

Atomic spin logic



STM used to form linear chains of atoms separated ~0.9 nm: AF RKKY interactions

End atoms act as gates for the output atom

Four couplings: J_{isl} (larger), J_l, J_α, J_β

- Inputs addressed using H_{ext} (different coercivity)
- Transmission of information via RKKY interactions, from input to gates
- Output state determined by gates and couplings:
  - If $J_l > J_\alpha > J_\beta$ or $J_l > J_\alpha > J_\beta$: output only determined by dominant chain
  - If $J_\alpha > J_\beta > J_l$: cross-talk between spin leads
  - If $J_l > J_\alpha = J_\beta$: logic operations

	α, β odd	α, β even
$\vec{B}_{bias} \uparrow\uparrow \vec{M}_{tip}$	OR	NAND
$\vec{B}_{bias} \uparrow\downarrow \vec{M}_{tip}$	AND	NOR

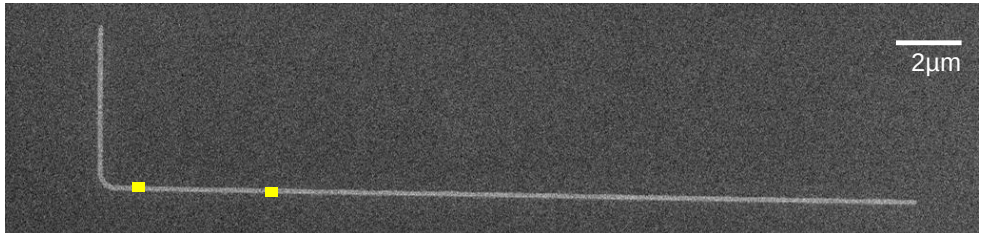
[Khajetoorians et al, Science 332, 1062 (2011)]

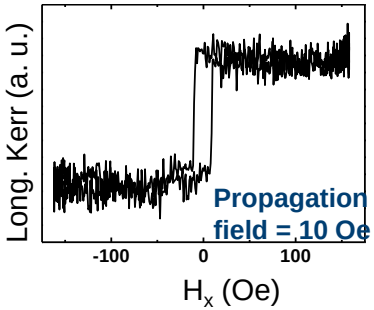
Outline

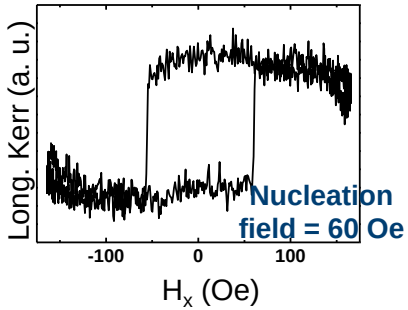
1. Coupled nanomagnets
2. Domain-walls in nanowires
3. MRAM & CMOS

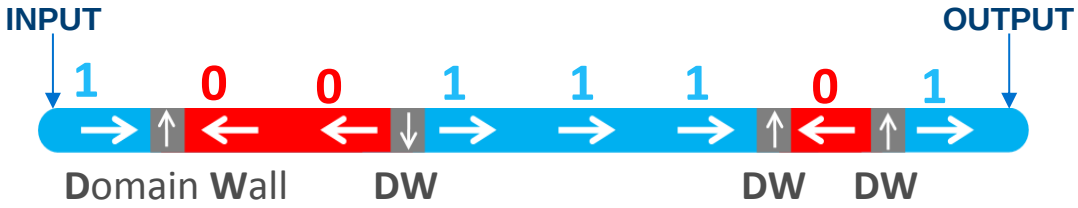
Nanowires: conduits for domain walls

~100-200 nm wide, ~10 nm thick Permalloy nanowire

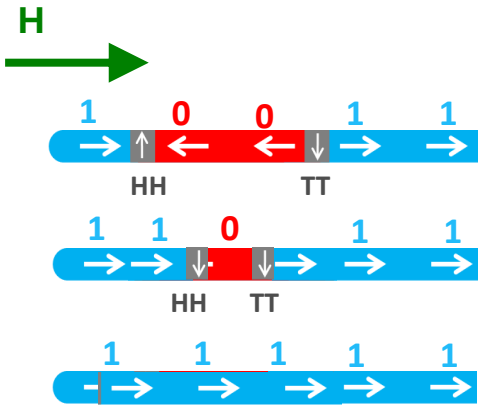








Bits: two possible directions, with DWs separating bits

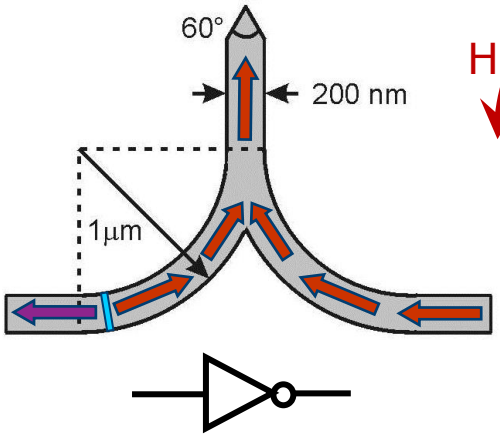


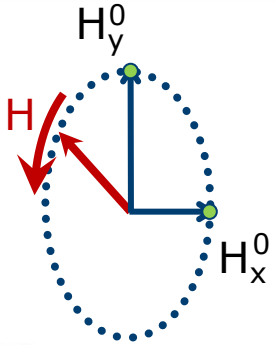
Under external H, "0" & "1" move in opposite directions!
How to get unidirectional motion?:

- **Bends & rotating fields: FULL LOGIC**
- **STT motion: RACETRACK**
- **Asymmetric pinning site potentials**

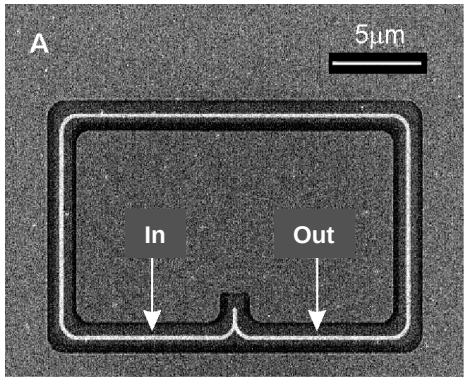
[Ono et al, Science 284, 468 (1999);
Cowburn et al, JAP 91, 6949 (2002)]

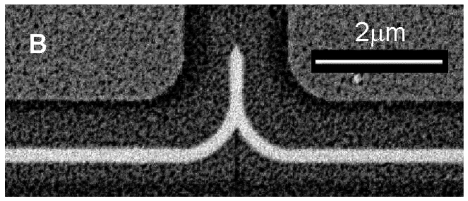
NOT gate

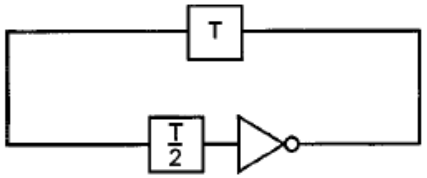


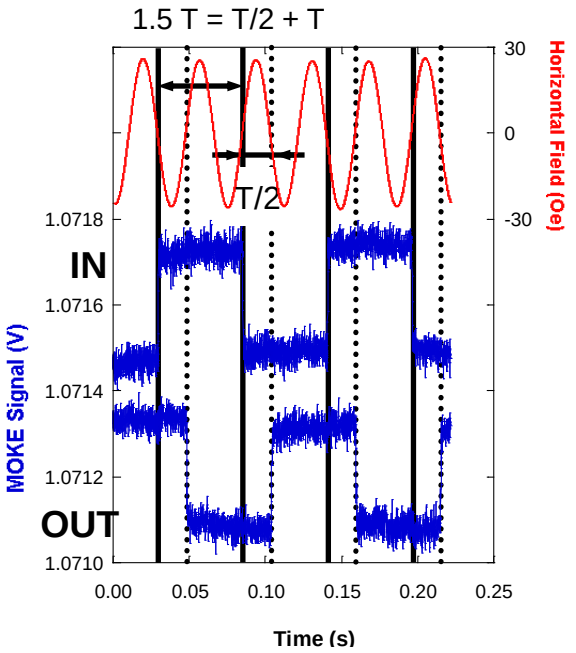


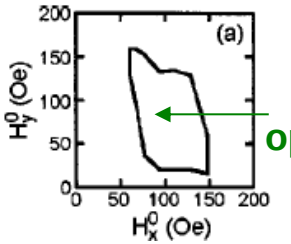
Elliptical H: Rotation sense defines direction motion of DWs



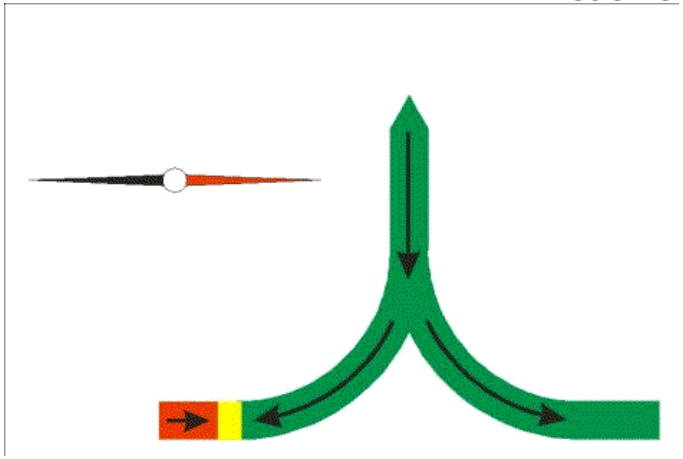






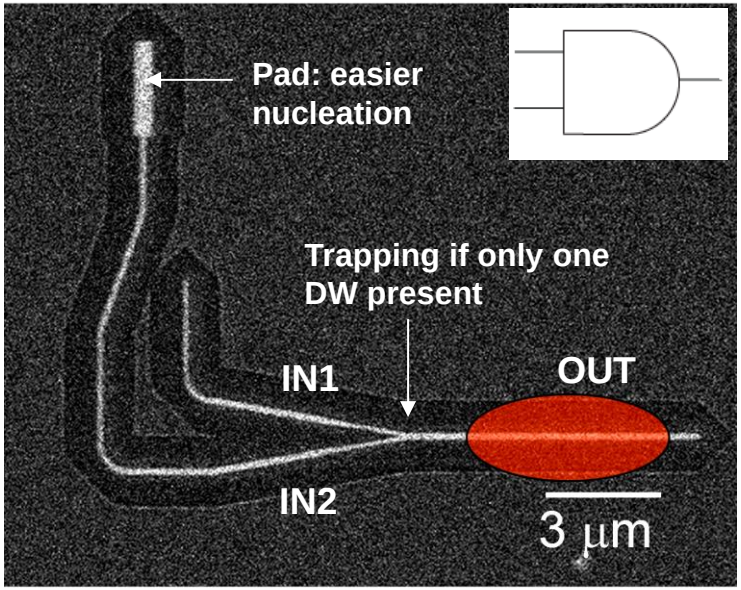


Good operation

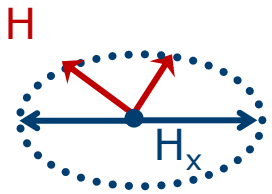


[Allwood et al, Science 296, 2003 (2002); JAP 95, 8264 (2004); Zhu et al, APL 87,

AND/OR gate

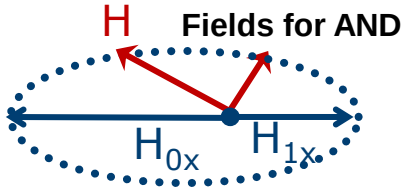


In1	In2	Out
0	0	0
0	1	0/1
1	0	0/1
1	1	1



Depinning from the cross only when two DWs are present

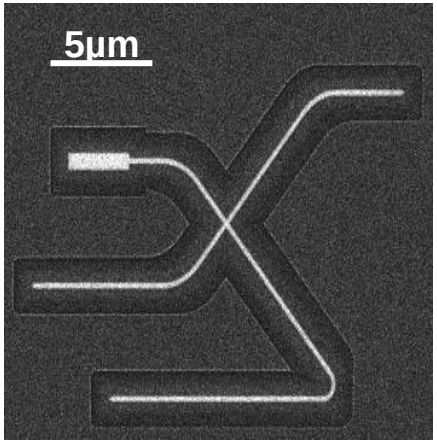
PROBLEM: (0,1) & (1,0) are undefined→ OUT will have the previous value
SOLUTION:
- **Reinitialise system to "0" every cycle**
- **Offset in H_x, favouring either 0-state (AND) or 1-state (OR)**

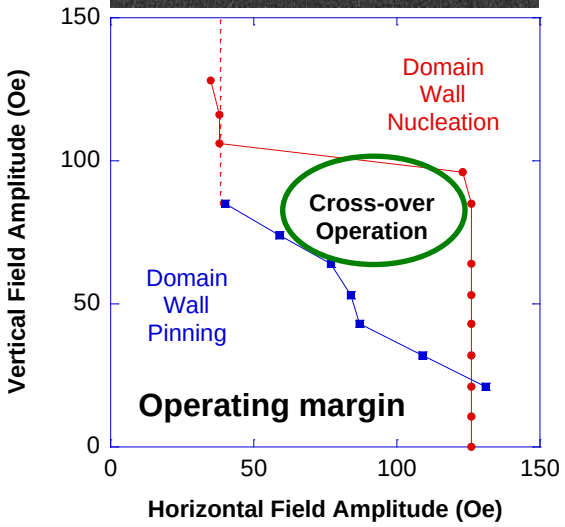


[Faulkner et al. IEEE Trans. Mag. 39, 2860 (2003); Allwood et al, Science 309, 1688 (2005)]

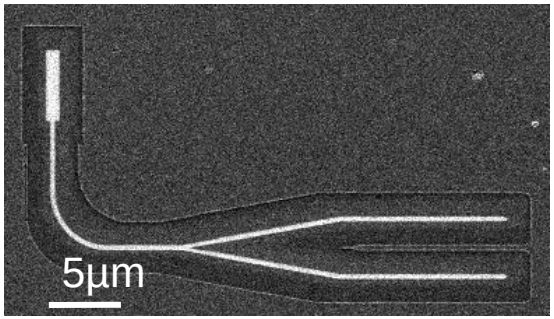
CROSS-OVER & FAN-OUT gates

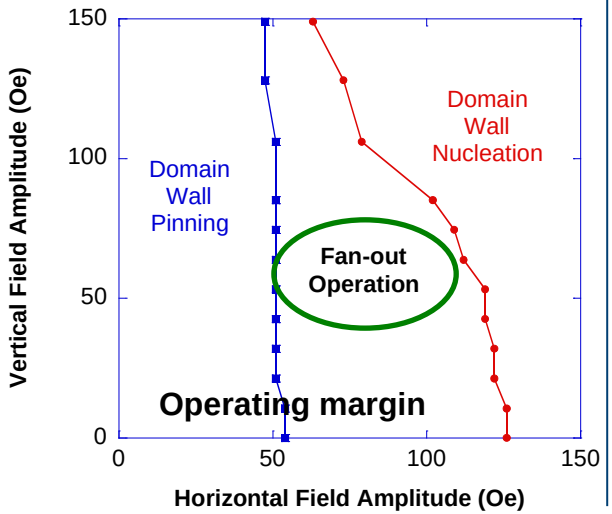
CROSS-OVER



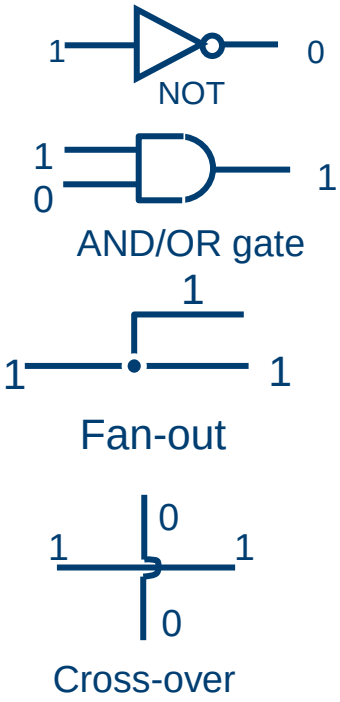


FAN-OUT





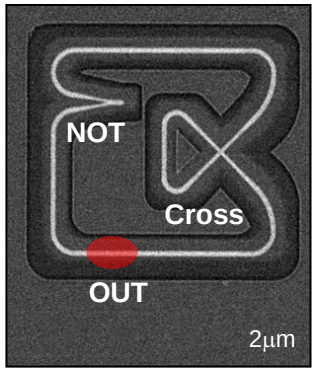
FULL SET OF LOGIC GATES: any complex logic operation possible!!

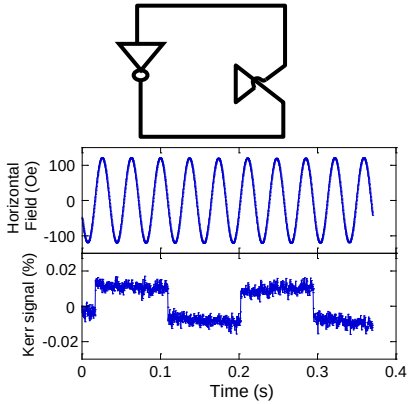


[Allwood et al, Science 309, 1688 (2005);
O'Brien et al, Phil. Trans. R. Soc. A 370, 5794 (2012)]

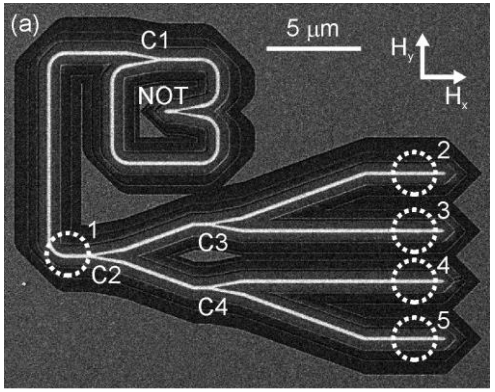
Complex logic circuits

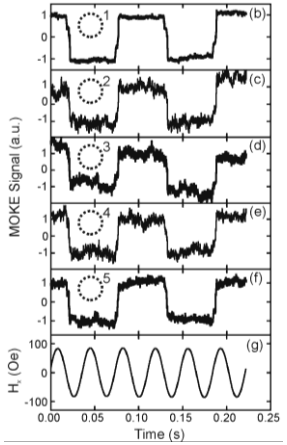
NOT + CROSS-OVER



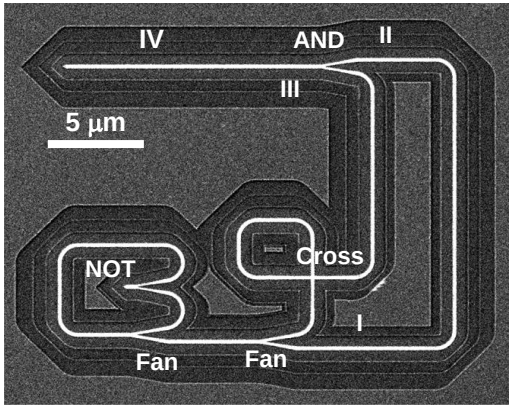


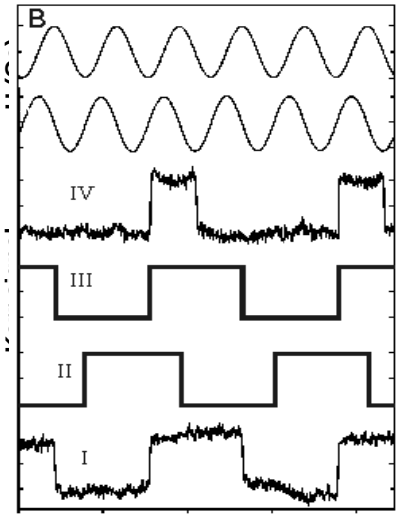
MULTIPLE FAN-OUT (DW CLONING)





4-ELEMENT NANOCIRCUIT





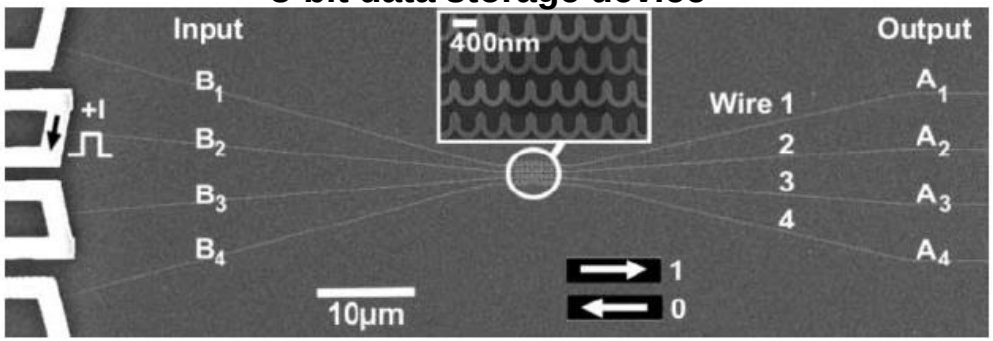
Circuit operation:

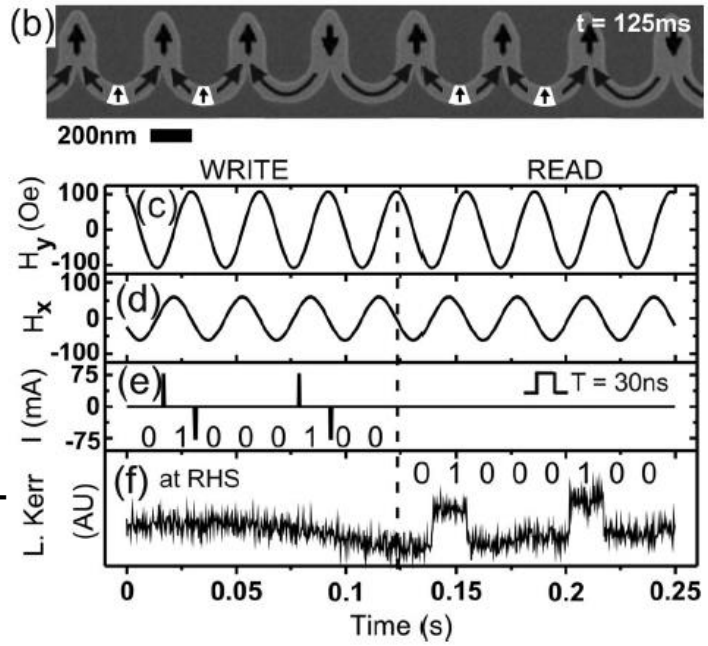
- Apply global field. Pads and corners act as nucleation areas
- Run external field, erasing unwanted DWs before normal operation
- Operation: external rotating H as power supply & CLK
- Readout using MOKE

[Allwood et el, JAP 101, 024308 (2007); Science 309, 1688 (2005); Hrcak et al, Phil. Trans. R. Soc. A 369 (2011)]

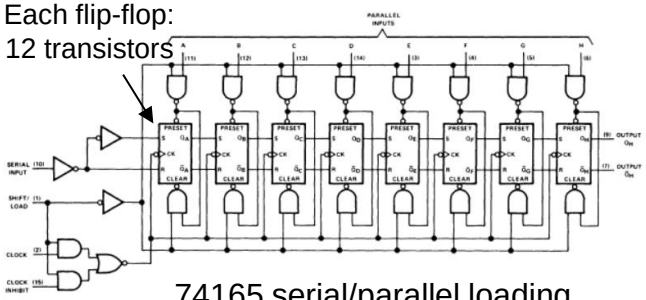
NOT-gate chain: bi-directional shift register

8-bit data storage device





Each flip-flop:
12 transistors



74165 serial/parallel loading
8-bit shift register

Chain of “N” NOT-gates: shift register, with OUT after=N/2 periods

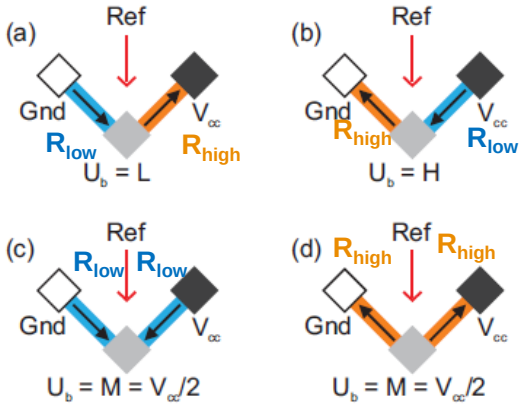
Strip line to generate DWs using local fields and MOKE/MR readout

Bi-directional flow of information!

[Allwood et al, Science 296, 2003 (2002); O’Brien et al, APL 95, 232502 (2009); Zeng et al, APL 96, 262510 (2010)]

Multi-turn counter using NOT gates

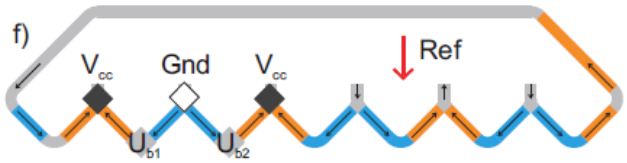
GMR & Wheatstone ½ bridge



GMR to control DW position:

- Wheatstone bridge to compensate for T changes
- GMR values depend on angle with reference layer
- 3 possible intermediate voltages U_b

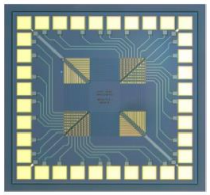
Multi-turn counter based on binary/co-prime counting loops



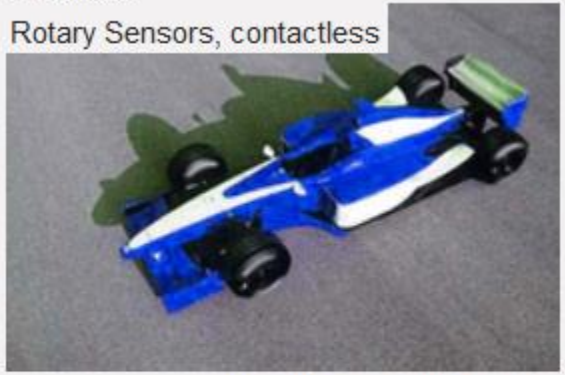
- Place a specific amount of DWs into the circuit
- Apply rotating fields N times (unknown)
- From voltage values: determine N: high-N non-volatile multi-counter

novotechnik
Siedle Group

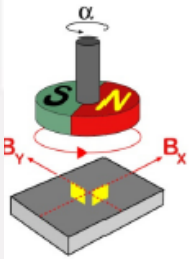
http://www.novotechnik.de



Product:
Rotary Sensors, contactless



The non-contacting multi turn sensor RSM2800 is well suited to be used in applications requiring to measure more than 360 degrees, for example in steering angle measurement applications.



[Mattheis et al, JAP 111, 113920 (2012);
Weis et al, Meas. Sci. Technol. 24, 082001 (2013)]

Current-induced domain wall motion

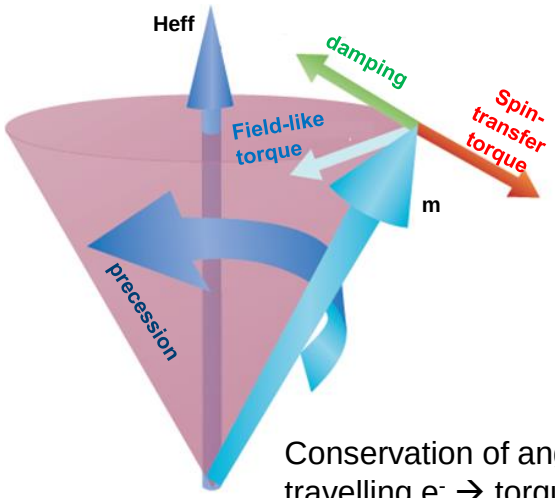
Landau–Lifshitz–Gilbert–Slonczewski equation:

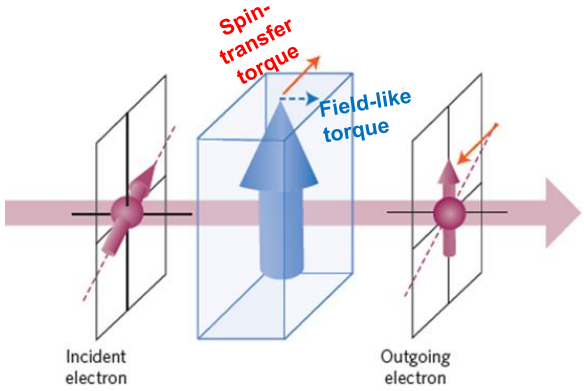
$$\dot{\vec{m}} = -\gamma_0 \vec{m} \times \vec{H}_{eff} + \alpha \vec{m} \times \dot{\vec{m}} + \vec{\tau} \; ; \text{ with } \vec{\tau} = -(\vec{u} \cdot \vec{\nabla})\vec{m} + \beta \vec{m} \times (\vec{u} \cdot \vec{\nabla})\vec{m}$$

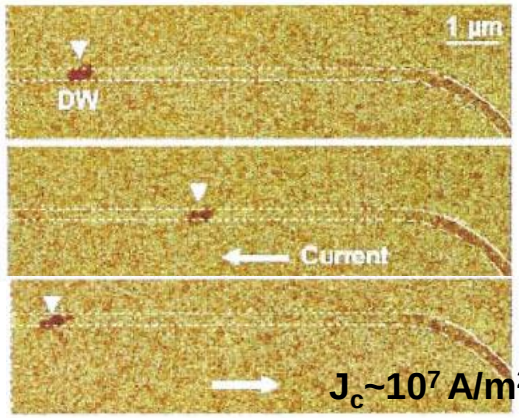
precession | damping | current-induced torques | adiabatic (spin-transfer) torque | non-adiabatic (field-like) torque

$$\vec{u} = \vec{j} g P \mu_B / (2eM_s)$$

$$\beta = (\lambda_J / \lambda_{SF})^2$$





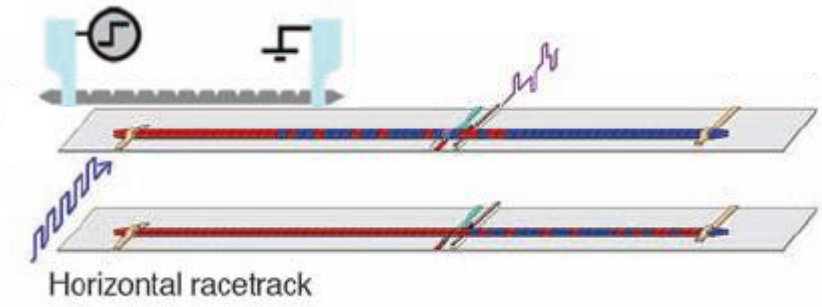


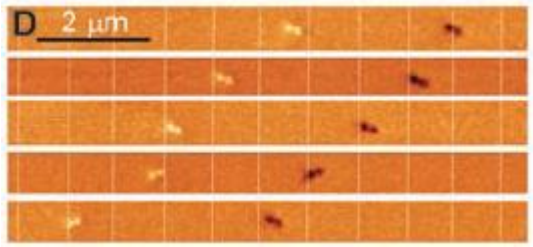
Conservation of angular momentum: change of momentum in travelling e^- → torque in magnetisation of the material → DW motion

- DWs move in the (contrary) direction of current
- Torque values and relative magnitude depend on material & DW structure
- Other torques can also be present : Spin-Hall/Rashba

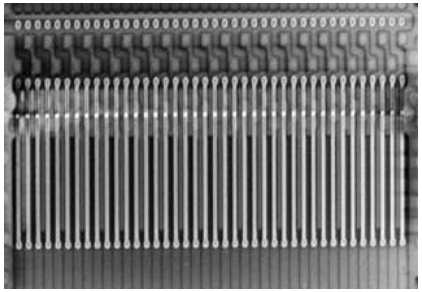
[Beach et al. JMMM 320, 1272 (2008); Braatas et al, Nature Materials 11, 372 (2012); Yamaguchi et al, PRL 92, 077205 (2004)

Racetrack memory

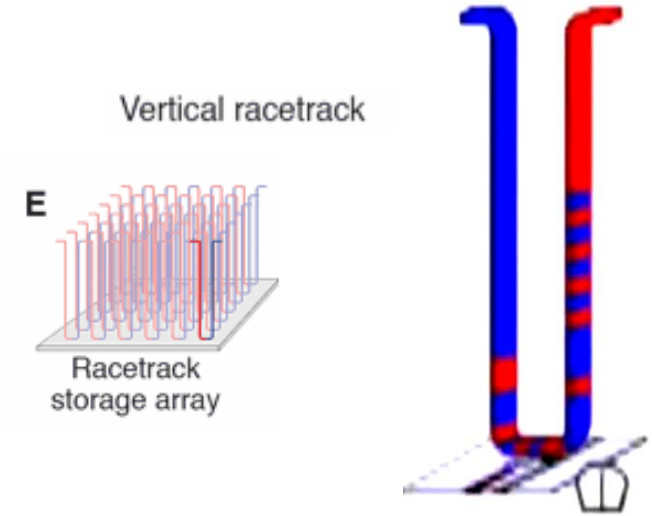


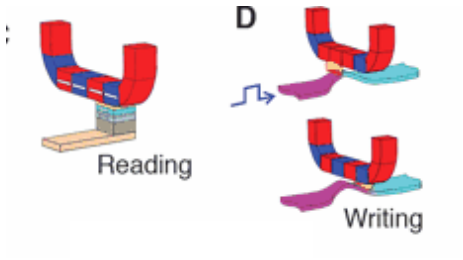


Motion of two DWs under current pulse =26 mA, 14ns



Horizontal racetrack memory prototype-2011 (Permalloy)



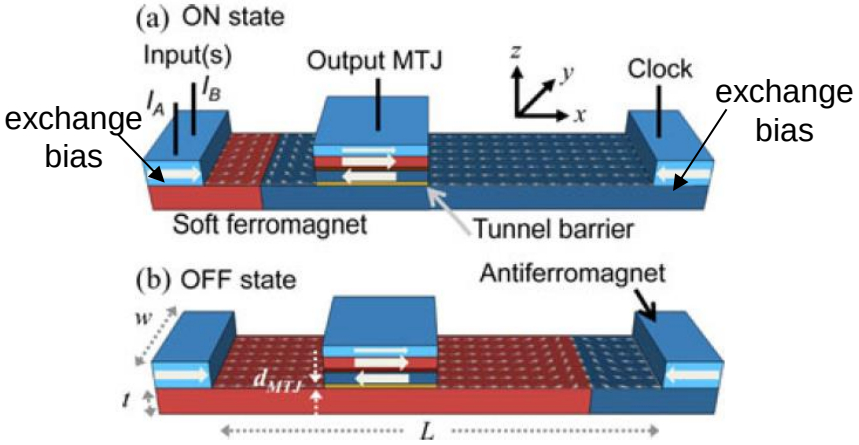


Arrays of nanowires with notches, where multiple domain walls are stored and moved using CIDWM: shift register, full electrical control

Vertical racetrack memory proposed: not implemented ye due to difficulty to pattern vertical nanowires

[Parkin et al. Science 320, 190 (2008); IBM, IEDM (2011); Fernández-Pacheco et al, Sci. Rep. 3, 1492 (2013)]

Domain wall logic & racetracks



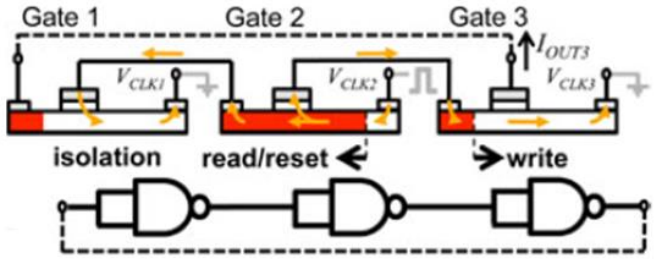
- Always one DW in the device using exchange bias with edge electrodes
- Small pinning sites to avoid undesired DW motion
- CIDWM shifts DW to left/right of MTJ using I_A+I_B

OPERATION:

- WRITE: Current applied to inputs I_A, I_B
- READ/ERASE: Voltage applied to CLK to measure TMR/motion of DW to initial position

LOGIC GATE:

- NAND: I_A, I_B < I_C, but I_A+I_B> I_c if both ON
- NOR: I_A, I_B > I_C
- AND/OR by reversing fixed layer of MTJ



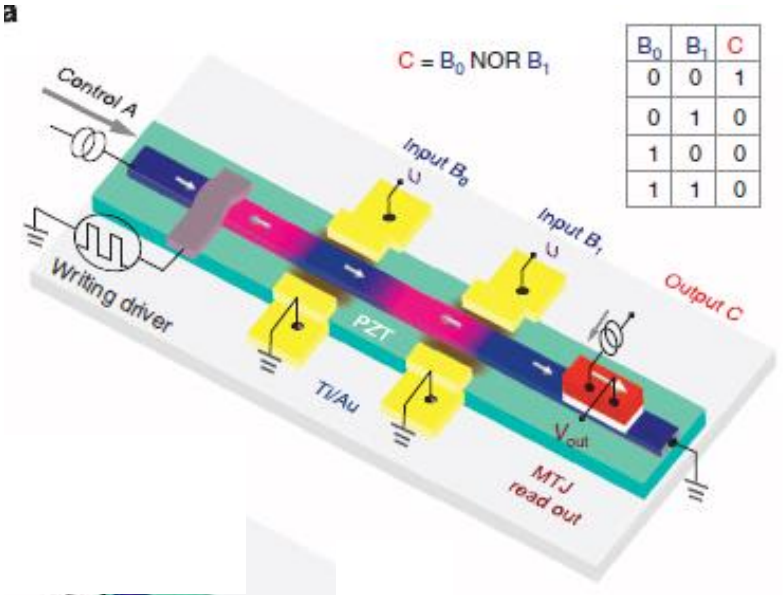
Shift register formed by 3 NAND gates in series

PERSPECTIVES:

- Speed: 1GHz maximum
- Energy: 100 times more efficient than CMOS (PMA)
- Scaling: 10 nm

[Curriban et al. IEEE Magn. Lett. 3, 3000104 (2012)]

Strain-controlled domain wall logic



B_0	B_1	C
0	0	1
0	1	0
1	0	0
1	1	0

- DW injected using strip line
- Stress created by piezoelectric material on FM can trap a DW
- TMR value will be 1 or 0 if DW arrived or not

OPERATION:

- Inject DW
- WRITE: Voltages to inputs B_0, B_1 & magnetic field for DW motion are applied
- READ: Voltage applied to MTJ to measure TMR
- ERASE: reset magnetization of nanowire

NOR GATE:

DW will get trapped if any of the two inputs is set to “1”

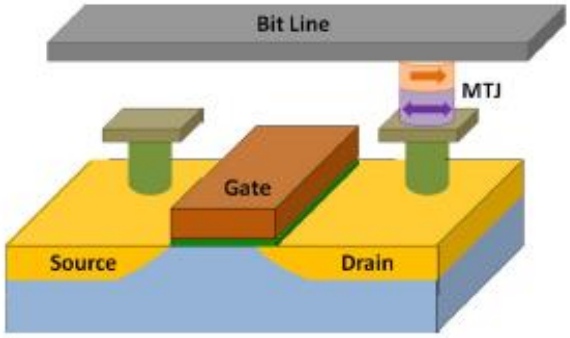
NAND if fixed & free layers of MTJ were initially paralel

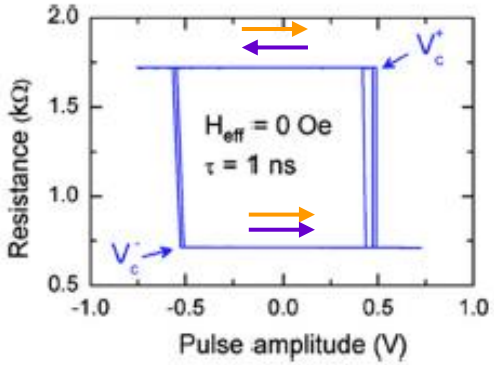
[Lei et al. Nat. Comm. 4, 1378 (2012)]

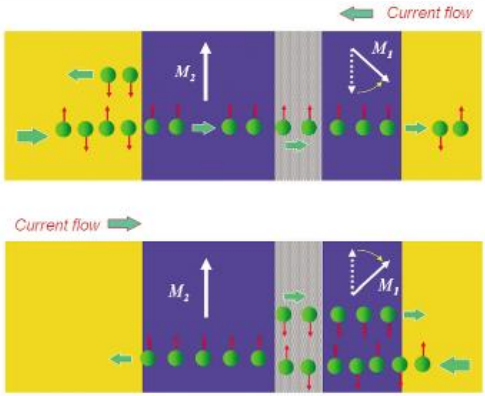
OUTLINE

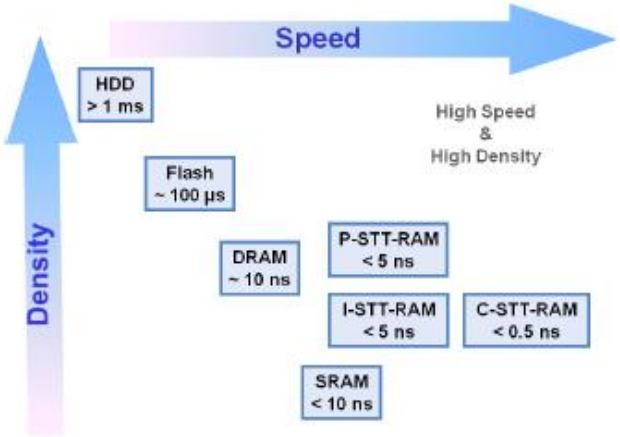
1. Coupled nanomagnets
2. Domain-walls in nanowires
3. MRAM & CMOS

MRAMs









	Flash	STT-RAM
Write energy per bit	> 1 nJ	< 100 fJ
Speed	1 µs–1 ms	1–10 ns
Endurance	Low	Very High
Density (F^2)	4–8	8–20
Maturity	Product	R&D

HITACHI intel FUJITSU SAMSUNG NEC EVERSPIN TOSHIBA GRANDIS

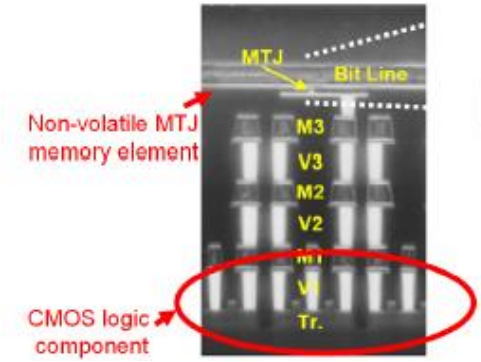
STT-MRAM

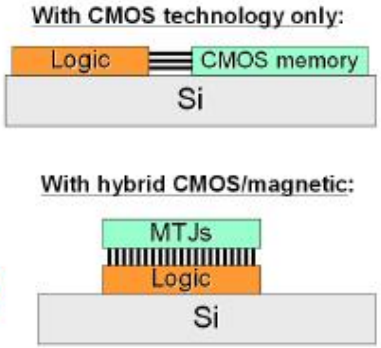
Non-volatile, high-density, high-speed memory

64MB DDR3 SDRAM (2013)

[Zhu, Materials Today 9, 36 (2006)
Wang et al, SPIN 2, 1250009, (2012)]

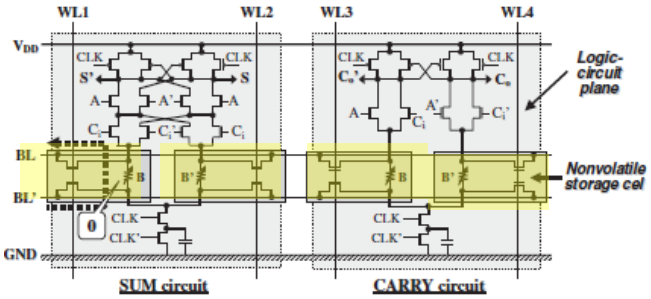
MRAMs/CMOS logic devices



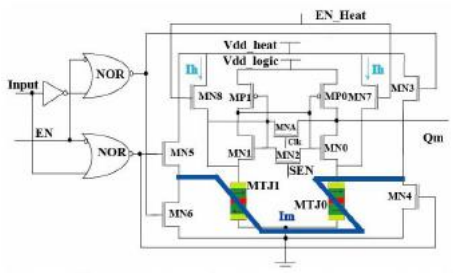


"Logic-in-Memory" architecture

Full-adder



Look-up table



Logic-In-Memory:

CMOS logic + MRAM memory, vertically connected:

- **Multiplication in number & shortening of connections LOGIC-MEMORY: simpler interconnection scheme**
- **Smaller footprint**
- **Higher speed**
- **Lower standby power consumption**
- **Lower dynamic power consumption: (power off unused blocks). Still need to reduce STT writing energy**

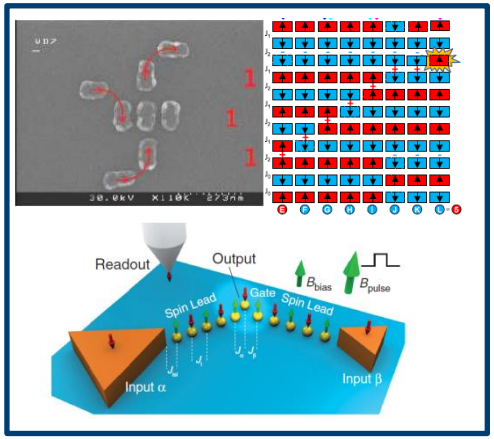
NEC + TOHOKU

1% of conventional systems

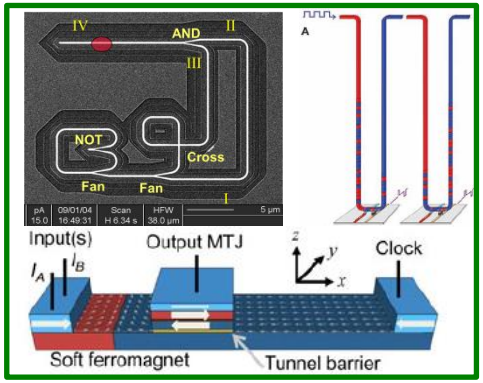
[Matsunaga et al, APEX. 1, 091301, (2008);
Prenat et al, ICCAD 978, 240 (2011)]

CONCLUSIONS

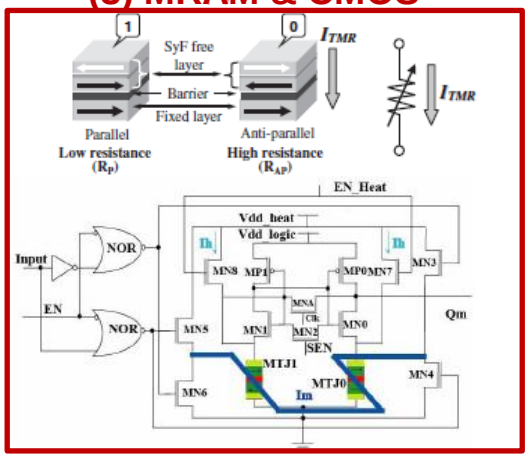
(1) COUPLED NANOMAGNETS



(2) DOMAIN WALLS & NANOWIRES



(3) MRAM & CMOS



SPINTRONIC LOGIC: Different alternatives to current CMOS-based technology

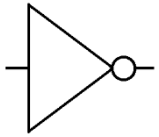
- Non-volatility
- Low power consumption
- Very competitive speeds
- Combination with storage devices: full electrical control via spin torques
- In spite of simple design, still far from beating transistors: lower power consumption + simple design (3D) are main advantages to exploit. In the meantime lots of fun physics!

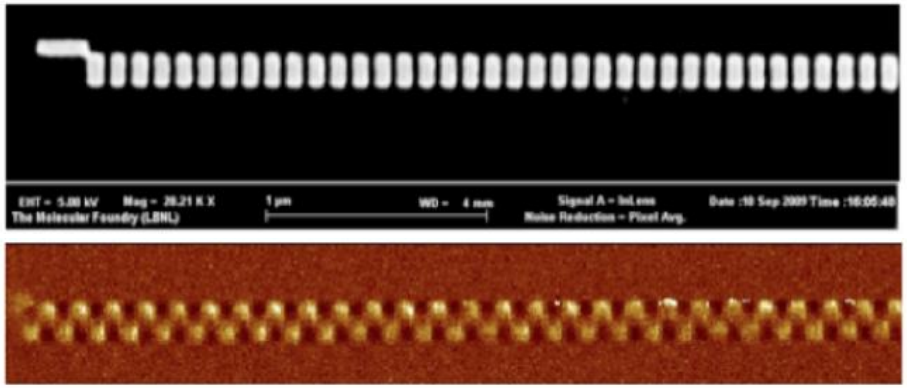
af457@cam.ac.uk
https://cambridge.academia.edu/amalio/

Extra slides

NOT & FAN-OUT gate

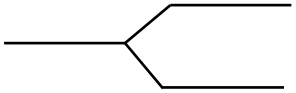
NOT GATE

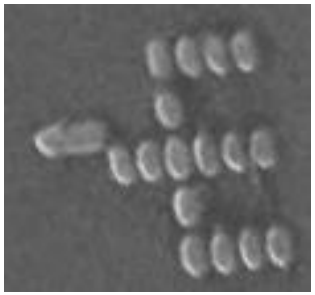


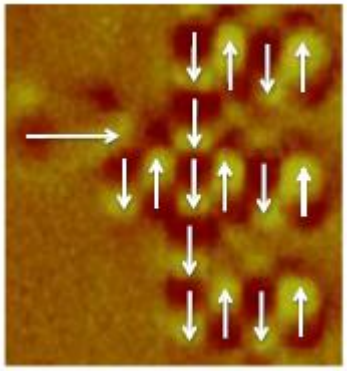


[David Carlton, ‘’Nanomagnetic logic’’, Thesis dissertation, University of Berkeley

FAN-OUT GATE





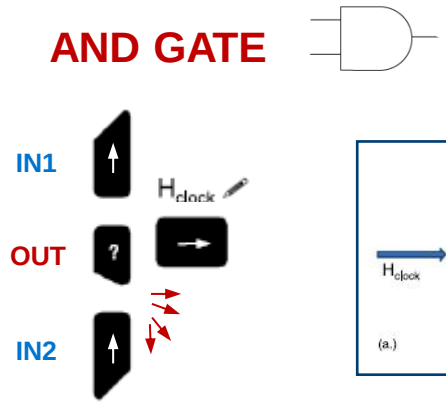


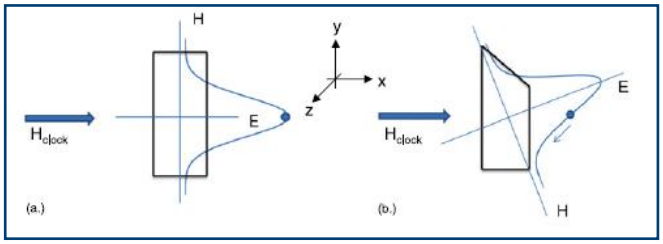
Transport of information along 3 identical lines

[Niemier et al, J. Phys.: Condens. Matter 23 493202 (2011)]

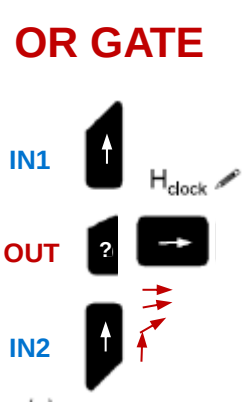
AND/OR gate

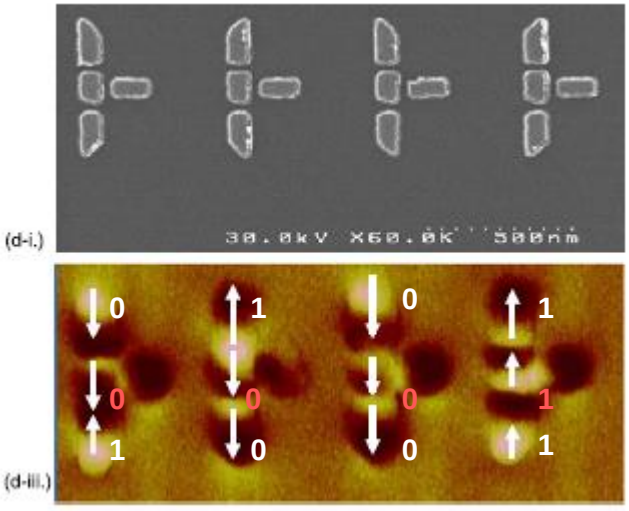
AND GATE

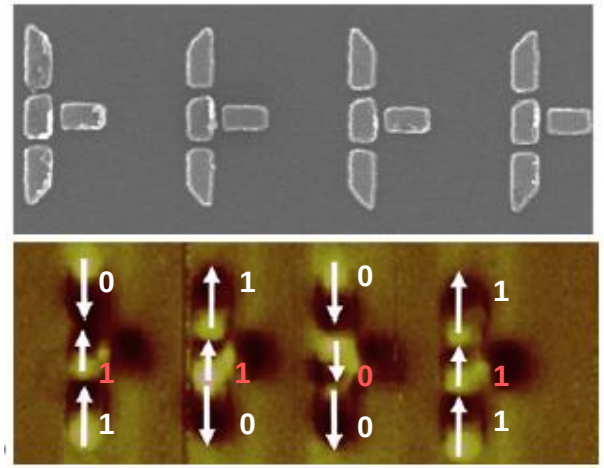




OR GATE

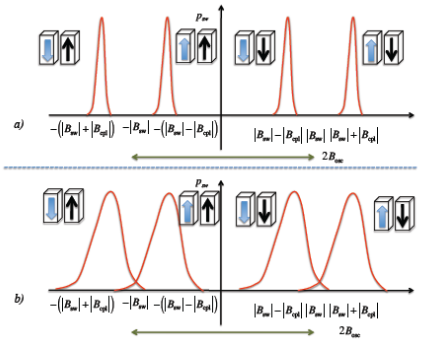




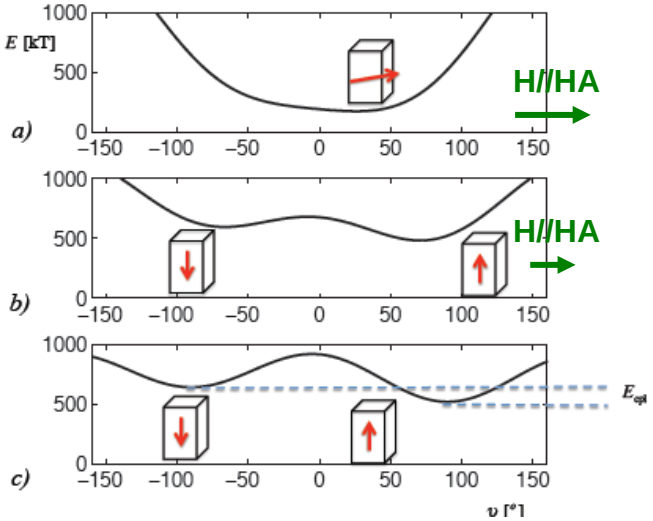


[Niemier et al, J. Phys.: Condens. Matter 23 493202 (2011)]

Hard vs easy axis processes



H//EA



H_{CLK} applied

Small barrier appears:
$P_{error} \sim e^{-Ecpl/KBT}$
(Ahrrenius switching)

Magnet ends in one of the two configurations

Adiabatic switching: orders of magnitude lower error than EA demagnetisation

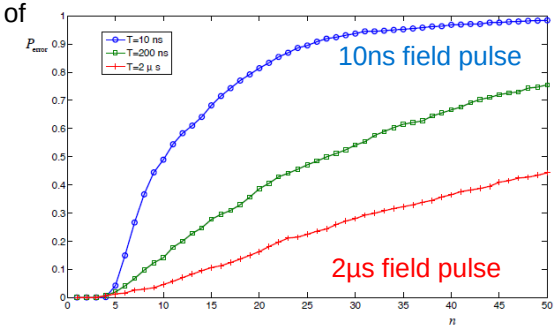


Fig. 6. The graph shows the probability of finding at least one ordering error in the first n dot of a 100 - magnet long nanomagnet wire. The duration of the clocking was T.

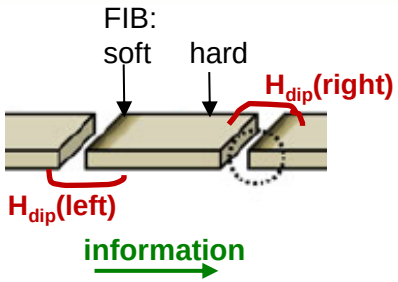
[Csaba et al, DOI:10.1109/IWCE.2010.5677954]

Modelling thermal fluctuations:

$$\frac{d\mathbf{M}^{(i)}(t)}{dt} = -\gamma \mathbf{M}^{(i)}(t) \times \mathbf{H}_{\text{eff}}^{(i)}(t) - \frac{\alpha\gamma}{M_s}\left[\mathbf{M}^{(i)}(t) \times \left(\mathbf{M}^{(i)}(t) \times \mathbf{H}_{\text{eff}}^{(i)}(t)\right)\right]$$

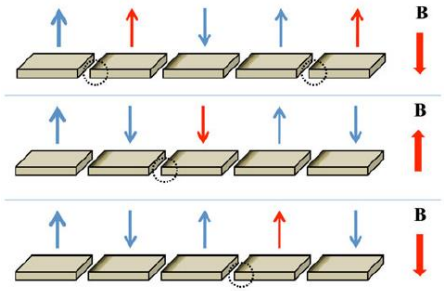
$$\mathbf{H}_{\text{therm}} = \frac{1}{\sqrt{V\Delta t}}\sqrt{\frac{2kT\alpha}{\mu_0\gamma M_s}}\mathbf{g}(t) \qquad \mathbf{H}_{\text{eff}}^{(i)} = -\mathbf{N}^{(i)}\mathbf{M}^{(i)} + \sum_{j=\text{neighbors}} \mathbf{C}^{(ji)}\mathbf{M}^{(j)} + \mathbf{H}_{\text{ext}}^{(i)} + \mathbf{H}_{\text{therm}}^{(i)}.$$

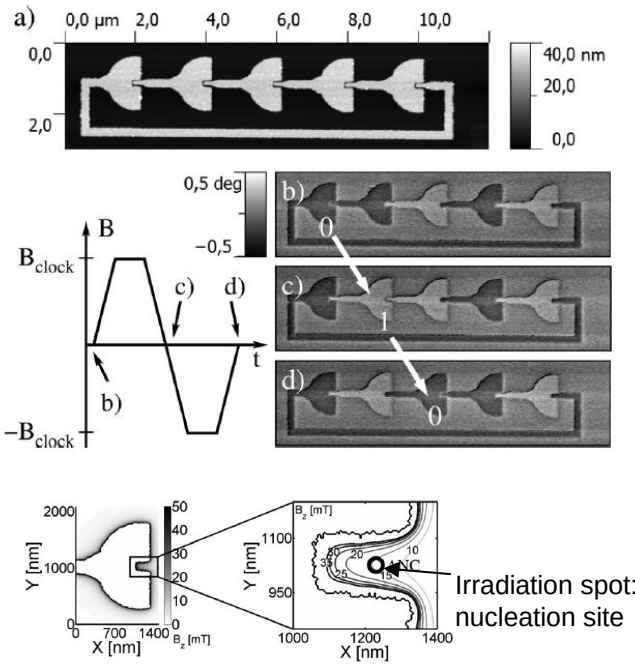
FIB-irradiated perpendicular materials



Anisotropy in PMA can be tuned by FIB irradiation

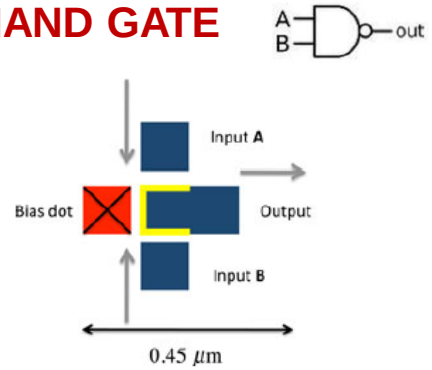
Asymmetric FIB creates propagation directionality



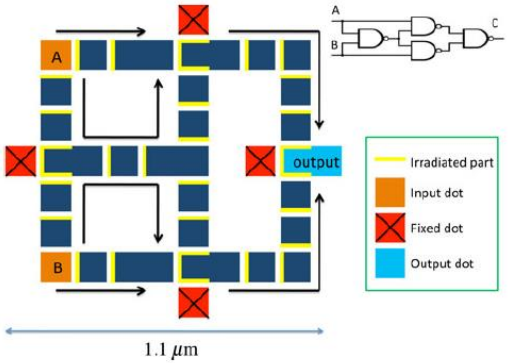


Soliton moved one step right every half H-cycle

NAND GATE

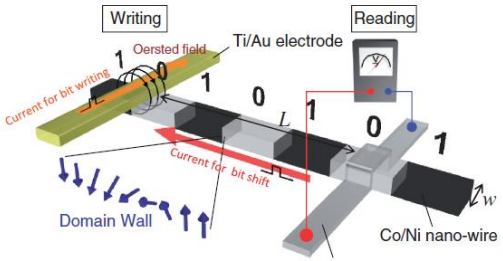


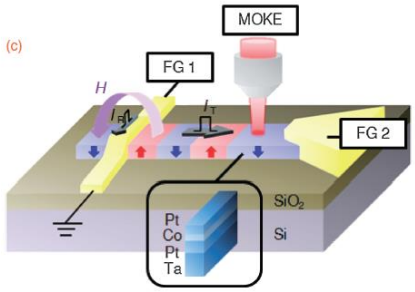
XOR GATE

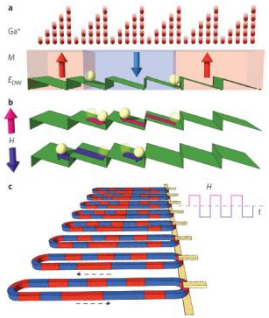


[Ju et al, IEEE Trans. Nano 11, 97 (2012); Kiermaier, J. Appl. Phys. 113, 17B902 (2013)]

Perpendicular materials

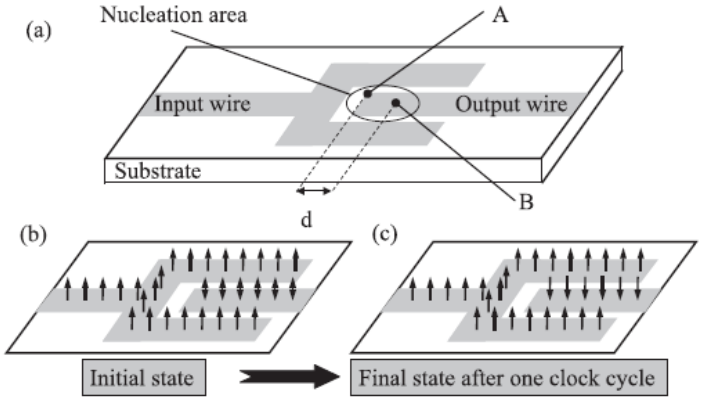






PMA materials (Pt/Co, Co/Ni, Pt/CoFeB/MgO, Pt/Co/AlO_x) have narrower DWs: higher storage density & lower J_c for DW motion

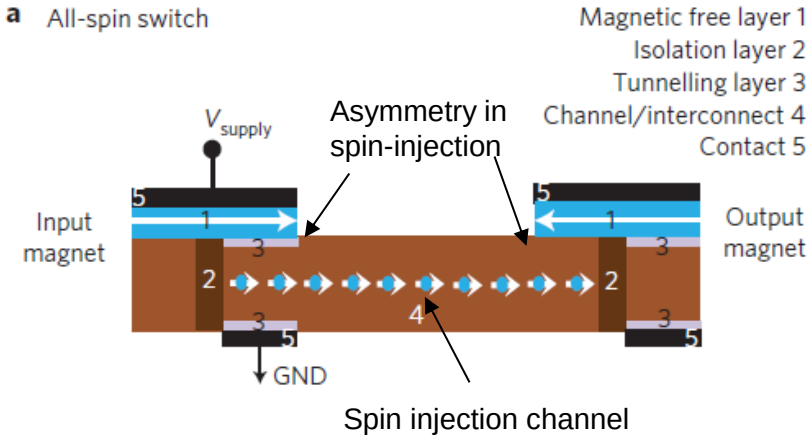
LOGIC WITH PMA MATERIALS

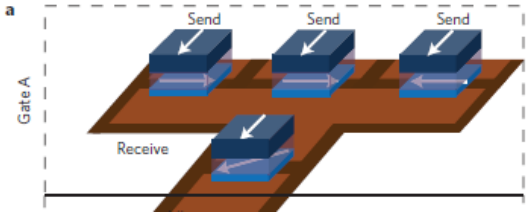


- Application of out-of-plane fields changes input state
- Output determined by stray field from both arms

[Kim et al. APEX 3, 083001 (2010); Chiba, et al. APEX 3, 073004 (2010); Franken et al, Nat. Nano 7, 499 (2012); Jaworowicz et al, Nanotechnology 20, 215401 (2009)]

All-spin logic proposal





AND/OR - NAND/NOR GATES

MTJs incorporated for readout

Two inputs+ reference determine output

All-Spin logic: transform S-signal into charge.

No H needed, all S-based

- Input storing information addressed using STT
- Spin current flows along a S-coherence channel: determines final state of output
- If V_{supply} > 0: Extracts majority spins → output ⊥ input: **NOT**
  < 0: Injects majority spins → output // input: **DATA COPY**

[Behin-Aein et al, Nat. Nano. 5, 266 (2010)]