Optimized interchip spacing control in flip chip geometry.

In order to use quantum computing to tackle classically intractable problems, quantum processors must grow to larger scales. But routing control lines to an increasing number of qubits is not feasible in current planar architectures.

This problem can be address by using 3D-integration techniques such as flip chip bump bonding. One challenge arising from this new technology is achieving an unerring vertical placement of the chips. In a flip chip assembly, key circuit parameters, such as capacitances and inductances, are determined by the distance separating the bonded chips. However, during bonding, chips may move or tilt because of irregularities, eventually affecting the interchip gap.

In this talk/presentation we present our strategy to mitigate planar displacements and chip slanting under a 1um tolerance. It includes the optimization of an indium evaporation resist-mask, for a precise and uniform indium bump fabrication, as well as the development of epoxy-based spacers for an accurate and reproducible control of the spacing.