Investigating loss in superconducting circuits

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Superconducting qubits are current hot candidates for delivering on the promise of quantum computation. However, their implementation is not without challenges. Quantum information stored in a qubit has a finite lifetime before it loses coherence. For superconducting qubits to be able to sustain the fragile quantum information in a coherent state sufficiently long so that a meaningful number of logical gates can be executed, it is vital to examine the sources of decoherence and to eliminate them.

The nature of the sources of coherence loss in quantum circuits is a topic of ongoing debates. In this work we investigate the parasitic two-level systems (TLS) that compete with our devices for photons, as well as shine some light on other losses that may limit performance once TLS loss has been mitigated.

As a proxy for these investigations we use superconducting coplanar waveguide resonators (CPWs), which are subject to many of the same loss sources a qubit would, but are faster to fabricate and characterize. We approach this problem from two angles - device geometry and surface engineering. Manipulating device geometry, we can quantify the relative effect each interface of the CPW resonator has on the total loss. With surface engineering, we can target a given interface in order to mitigate the specific type of loss it entails.

We design, fabricate and characterize resonators and qubits using aluminium on silicon in order to further investigate the nature of TLS. We vary the deposition conditions of the metal, as well as surface treatments, and draw conclusions for the participation of TLS loss to the total loss of the circuits at low temperatures. Varying the absolute size of the CPWs, as well as the ratio of the CPW center conductor to its gap to ground, we can get a more accurate picture of the various loss contributions.